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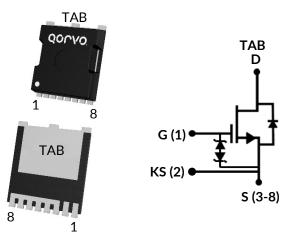
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### DATASHEET

### UJ4C075033L8S



Part Number	Package	Marking
UJ4C075033L8S	MO-229	UJ4C075033



### Silicon Carbide (SiC) Cascode JFET -EliteSiC, Power N-Channel, TOLL, 750 V, 33 mohm

Rev. D, January 2025

### Description

The UJ4C075033L8S is a 750V,  $33m\Omega$  G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal re-design when replacing Si IGBTs, Si superjunction devices or SiC MOSFETs. Available in the space-saving MO-229 package which enables automated assembly, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

#### Features

- On-resistance  $R_{DS(on)}$ : 33m $\Omega$  (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q<sub>rr</sub> = 89nC
- Low body diode V<sub>FSD</sub>: 1.26V
- Low gate charge: Q<sub>G</sub> = 37.8nC
- Threshold voltage V<sub>G(th)</sub>: 4.8V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3
- MO-229 package for faster switching, clean gate waveforms

### **Typical applications**

- Line rectification and active-bridge rectification circuits in AC/DC front-ends
- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating





### **Maximum Ratings**

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V <sub>DS</sub>		750	V
Cata source veltage	V	DC	-20 to +20	V
Gate-source voltage	V <sub>GS</sub>	AC (f > 1Hz)	-25 to +25	V
Continuous drain current <sup>1</sup>		T <sub>C</sub> = 25°C	44	А
Continuous drain current	ID	T <sub>C</sub> =100°C	33	А
Pulsed drain current <sup>2</sup>	I <sub>DM</sub>	T <sub>C</sub> = 25°C	132	А
Single pulsed avalanche energy <sup>3</sup>	E <sub>AS</sub>	L=15mH, I <sub>AS</sub> =2.4A	43	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \le 500V$	200	V/ns
Power dissipation	P <sub>tot</sub>	T <sub>C</sub> = 25°C	205	W
Maximum junction temperature	T <sub>J,max</sub>		175	°C
Operating and storage temperature	TJ, TSTG		-55 to 175	°C
Reflow soldering temperature	T <sub>solder</sub>	reflow MSL 1	260	°C

1. Limited by  $T_{J,max}$ 

2. Pulse width  $t_p$  limited by  $T_{J,max}$ 

3. Starting T<sub>J</sub> = 25°C

### **Thermal Characteristics**

Parameter Thermal resistance, junction-to-case	Symbol	Test Conditions	Value			Linita
			Min	Тур	Max	Units
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.56	0.73	°C/W



### Electrical Characteristics (T<sub>J</sub> = +25°C unless otherwise specified)

### Typical Performance - Static

Parameter	Cumple of	Test Conditions	Value			L Luckture
Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
Drain-source breakdown voltage	BV <sub>DS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =1mA	750			V
Total drain leakage current		V <sub>DS</sub> =750V,		2	20	
		V <sub>GS</sub> =0V, T <sub>J</sub> =25°C		Z	20	
	I <sub>DSS</sub>	V <sub>DS</sub> =750V,				μΑ
		V <sub>GS</sub> =0V, T <sub>J</sub> =175°C		20		
		V <sub>DS</sub> =0V, T <sub>J</sub> =25°C,		-	±20	μA
Total gate leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =-20V / +20V		6		
		V <sub>GS</sub> =12V, I <sub>D</sub> =30A,		33	41	mΩ
		TJ=25°C				
		V <sub>GS</sub> =12V, I <sub>D</sub> =30A,		- 7		
Drain-source on-resistance	R <sub>DS(on)</sub>	т <sub>ј</sub> =125°С		57		
		V <sub>GS</sub> =12V, I <sub>D</sub> =30A,		75		
		т <sub>ј</sub> =175°С		75		
Gate threshold voltage	V <sub>G(th)</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =10mA	4	4.8	6	V
Gate resistance	R <sub>G</sub>	f=1MHz, open drain		4.5		Ω

### Typical Performance - Reverse Diode

Parameter	Symbol Test Conditions		Value			Units	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Onits	
Diode continuous forward current <sup>1</sup>	I <sub>S</sub>	T <sub>C</sub> = 25°C			44	А	
Diode pulse current <sup>2</sup>	I <sub>S,pulse</sub>	T <sub>C</sub> = 25°C			132	А	
	M	V <sub>GS</sub> =0V, I <sub>S</sub> =15A, T <sub>J</sub> =25°C		1.26	1.42	Ň	
Forward voltage	V <sub>FSD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =15A, T <sub>J</sub> =175°C		1.59		V	
Reverse recovery charge	Q <sub>rr</sub>	$V_R$ =400V, I <sub>S</sub> =30A, $V_{GS}$ =0V, R <sub>G_EXT</sub> =50 $\Omega$		89		nC	
Reverse recovery time	t <sub>rr</sub>	di/dt=1100A/μs, T_=25°C		20.8		ns	
Reverse recovery charge	Q <sub>rr</sub>	$V_R$ =400V, I <sub>S</sub> =30A, $V_{GS}$ =0V, R <sub>G_EXT</sub> =50 $\Omega$		97		nC	
Reverse recovery time	t <sub>rr</sub>	di/dt=1100A/μs, Τ <sub>J</sub> =150°C		21.6		ns	





#### **Typical Performance - Dynamic**

Deventer	Cumple of	Test Canditions		Value		Units
Parameter	Symbol	Test Conditions	Min	Тур	Max	
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V		1400		
Output capacitance	C <sub>oss</sub>	f=100kHz		68		pF
Reverse transfer capacitance	C <sub>rss</sub>			2.5		
Effective output capacitance, energy	C	V <sub>DS</sub> =0V to 400V,		0.0		
related	C <sub>oss(er)</sub>	V <sub>GS</sub> =0V		83		pF
Effective output capacitance, time		V <sub>DS</sub> =0V to 400V,				_
related	C <sub>oss(tr)</sub>	V <sub>GS</sub> =0V		162		pF
C <sub>OSS</sub> stored energy	E <sub>oss</sub>	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V		6.6		μJ
Total gate charge	$Q_{G}$	– V <sub>DS</sub> =400V, I <sub>D</sub> =30A, –		37.8		nC
Gate-drain charge	$Q_{GD}$	$V_{GS} = 0V \text{ to } 15V$		8		
Gate-source charge	$Q_{GS}$			11.8		
Turn-on delay time	t <sub>d(on)</sub>	Notes 4, V <sub>DS</sub> =400V, I <sub>D</sub> =30A, Gate Driver =0V to +15V, Turn-on R <sub>G,EXT</sub> =1Ω,		11		- ns
Rise time	t <sub>r</sub>			21		
Turn-off delay time	t <sub>d(off)</sub>			126		
Fall time	t <sub>f</sub>	Turn-off $R_{G,EXT}$ =50 $\Omega$ ,		12		
Turn-on energy	E <sub>ON</sub>	inductive Load, FWD: same device with		176		μ
Turn-off energy	$E_{OFF}$	$V_{GS} = 0V$ and $R_G = 50\Omega$ ,		79		
Total switching energy	<b>E</b> <sub>TOTAL</sub>	T <sub>J</sub> =25°C		255		
Turn-on delay time	t <sub>d(on)</sub>	Notes 4,		11		
Rise time	t <sub>r</sub>	$V_{DS}$ =400V, $I_D$ =30A, Gate		22		
Turn-off delay time	$t_{d(off)}$	Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega$ , Turn-off $R_{G,EXT}=50\Omega$ , inductive Load, FWD: same device with		137		– ns
Fall time	t <sub>f</sub>			14		
Turn-on energy	E <sub>ON</sub>			189		
Turn-off energy	E <sub>OFF</sub>	$V_{GS} = 0V$ and $R_G = 50\Omega$ ,		86		μJ
Total switching energy	<b>E</b> <sub>TOTAL</sub>	т <sub>ј</sub> =150°С		275		]

4. Measured with the switching test circuit in Figure 23.





#### Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions		Value		
Palameter	Symbol		Min	Тур	Max	Units
Turn-on delay time	t <sub>d(on)</sub>	Notes 5 and 6,		12		
Rise time	t <sub>r</sub>	V <sub>DS</sub> =400V, I <sub>D</sub> =30A, Gate		22		
Turn-off delay time	t <sub>d(off)</sub>	Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega$ , Turn-off $R_{G,EXT} = 5\Omega$ ,		42		— ns
Fall time	t <sub>f</sub>			6		
Turn-on energy including R <sub>s</sub> energy	E <sub>ON</sub>	inductive Load,		178		
Turn-off energy including R <sub>s</sub> energy	E <sub>OFF</sub>	FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega$ ,RC snubber: $R_S=10\Omega$ and $C_S=100pF$ , $T_J=25^{\circ}C$		30		 
Total switching energy	E <sub>TOTAL</sub>			208		
Snubber R <sub>s</sub> energy during turn-on	E <sub>RS_ON</sub>			0.95		
Snubber R <sub>s</sub> energy during turn-off	E <sub>RS_OFF</sub>			1.43		
Turn-on delay time	t <sub>d(on)</sub>	Notes 5 and 6,		11		
Rise time	t <sub>r</sub>	V <sub>DS</sub> =400V, I <sub>D</sub> =30A, Gate		22		
Turn-off delay time	t <sub>d(off)</sub>	Driver =0V to +15V, Turn-on R <sub>G.EXT</sub> =1Ω,		42		ns
Fall time	t <sub>f</sub>	Turn-off $R_{G,EXT} = 5\Omega$ ,		7		
Turn-on energy including R <sub>s</sub> energy	E <sub>ON</sub>	inductive Load,		185		
Turn-off energy including R <sub>s</sub> energy	E <sub>OFF</sub>	FWD: same device with $V_{1} = 0$ and $P_{2} = 50$		31		
Total switching energy	E <sub>TOTAL</sub>	$-$ V <sub>GS</sub> = 0V and R <sub>G</sub> = 5 $\Omega$ , RC snubber: R <sub>S</sub> =10 $\Omega$ and		216		μJ
Snubber R <sub>s</sub> energy during turn-on	E <sub>RS_ON</sub>	C <sub>s</sub> =100pF,		1		
Snubber R <sub>s</sub> energy during turn-off	E <sub>RS_OFF</sub>	Т <sub>Ј</sub> =150°С		1.41		1

5. Measured with the switching test circuit in Figure 24.

6. In this table, the switching energies (turn-on energy, turn-off energy and total energy) presented include the device RC snubber energy losses.

### Typical Performance Diagrams

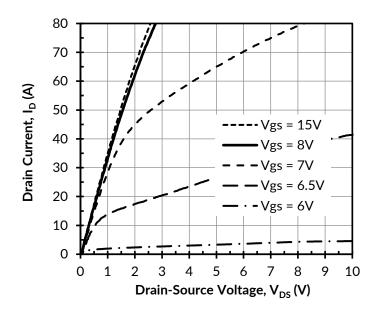
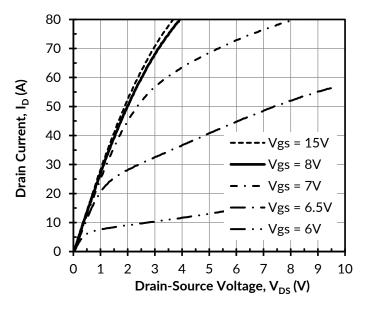


Figure 1. Typical output characteristics at T\_J = - 55°C, tp < 250 $\mu$ s



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Figure 2. Typical output characteristics at  $T_J = 25^{\circ}$ C, tp < 250 $\mu$ s

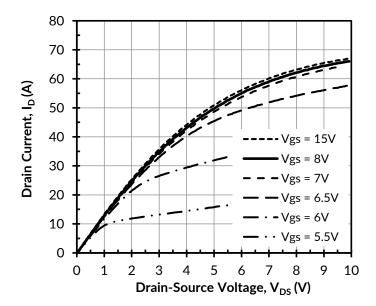


Figure 3. Typical output characteristics at T\_J = 175°C, tp < 250 $\mu$ s

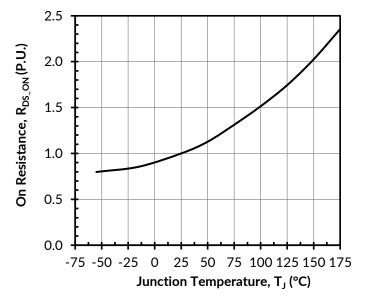


Figure 4. Normalized on-resistance vs. temperature at  $V_{GS}$  = 12V

### QOLVO

160

140

120

100

80

60

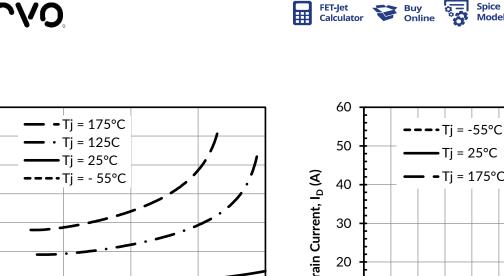
40

20

0

0

On-Resistance,  $R_{DS(on)}$  (m $\Omega$ )



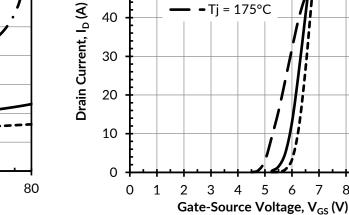


Figure 5. Typical drain-source on-resistances at  $V_{GS}$  = 12V

40

Drain Current, I<sub>D</sub> (A)

60

20

Figure 6. Typical transfer characteristics at  $V_{DS}$  = 5V

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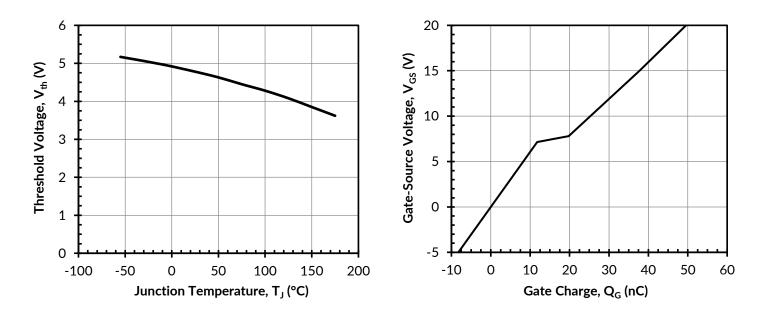
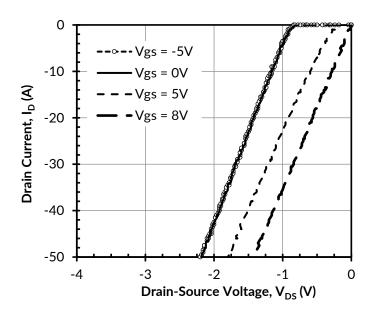


Figure 7. Threshold voltage vs. junction temperature at Figure 8. Typical gate charge at  $I_D$  = 30A  $V_{DS}$  = 5V and  $I_{D}$  = 10mA

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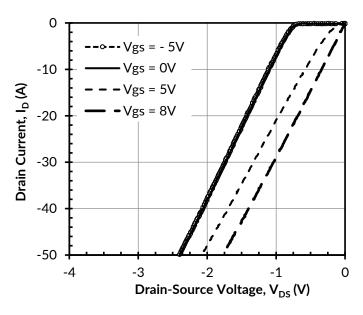


Figure 9. 3rd quadrant characteristics at  $T_{J} = -55^{\circ}C$ 

Figure 10. 3rd quadrant characteristics at  $T_J = 25^{\circ}C$ 

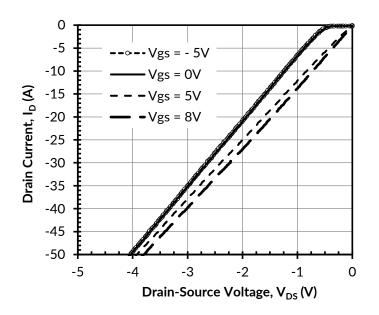


Figure 11. 3rd quadrant characteristics at  $T_J = 175^{\circ}C$ 

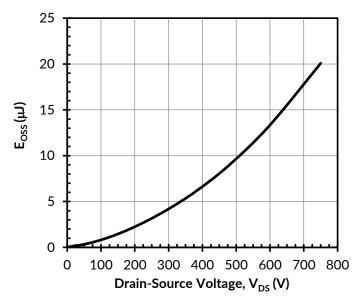


Figure 12. Typical stored energy in  $C_{OSS}$  at  $V_{GS}$  = 0V

### QOULO

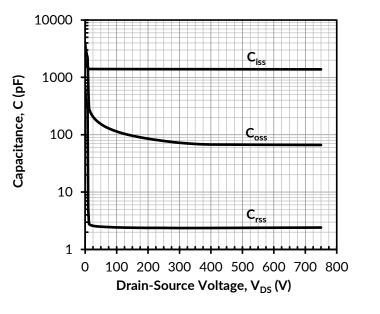
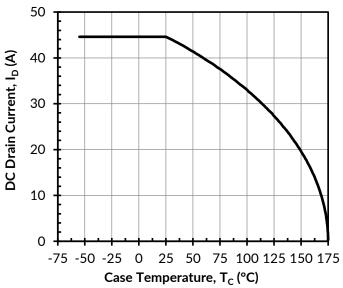


Figure 13. Typical capacitances at f = 100kHz and  $V_{GS}$  = 0V



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Figure 14. DC drain current derating

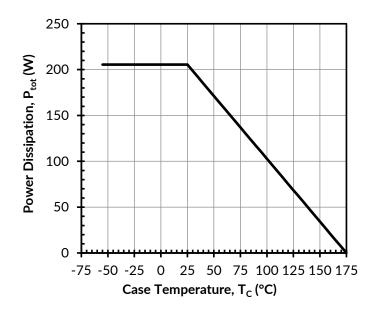


Figure 15. Total power dissipation

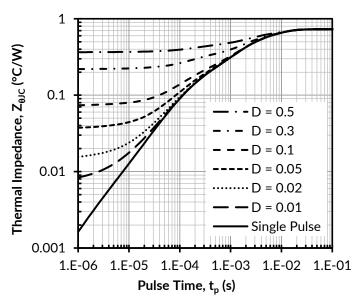


Figure 16. Maximum transient thermal impedance



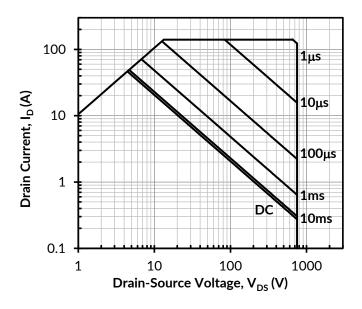


Figure 17. Safe operation area at  $T_C$  = 25°C, D = 0, Parameter  $t_p$ 

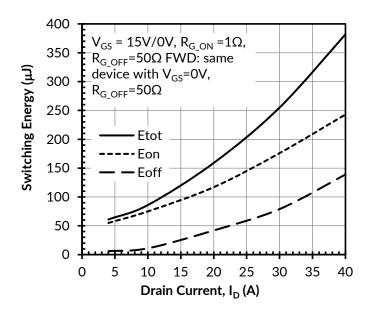


Figure 19. Clamped inductive switching energy vs. drain current at  $V_{DS}$  = 400V and  $T_J$  = 25°C

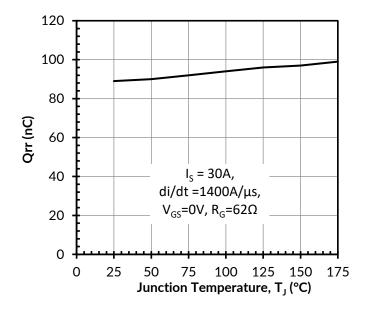


Figure 18. Reverse recovery charge Qrr vs. junction temperature at  $V_{DS}$  = 400V

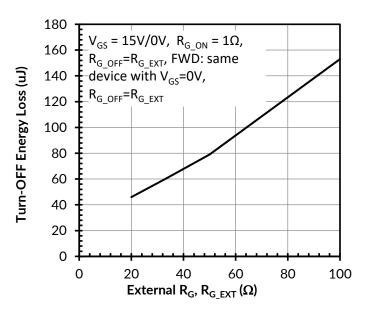
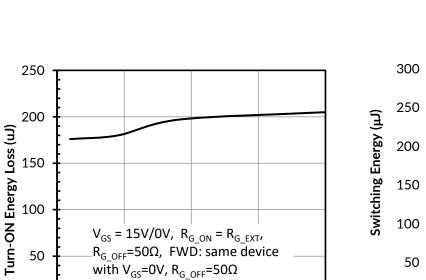


Figure 20. Turn-OFF clamped inductive switching energies vs.  $R_{G,EXT}$  at  $V_{DS}$  = 400V,  $I_D$  =30A, and  $T_J$  = 25°C

### QOUND



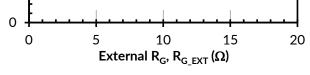


Figure 21. Turn-ON Clamped inductive switching energies vs.  $R_{G,EXT}$  at  $V_{DS}$  = 400V,  $I_D$  = 30A, and  $T_J$  = 25°C

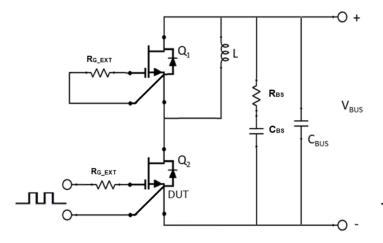
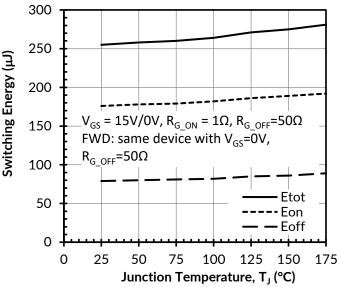


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ( $R_{BS}$  = 2.5 $\Omega$ ,  $C_{BS}$ =100nF) is used to reduce the power loop high frequency oscillations.



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Figure 22. Clamped inductive switching energy vs. junction temperature at  $V_{DS}$  = 400V and  $I_D$  = 30A

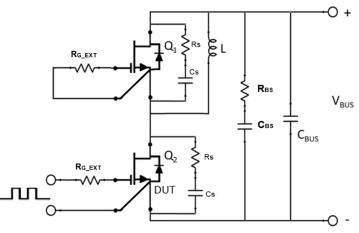
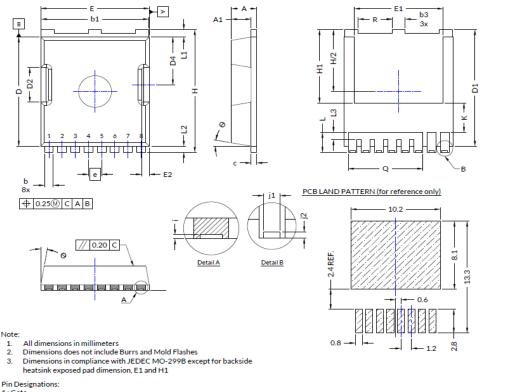


Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers ( $R_s$ =10 $\Omega$ ,  $C_s$  = 100pF) and a bus RC snubber ( $R_{BS}$  = 2.5 $\Omega$ ,  $C_{BS}$ =100nF).







	TO-LL							
SYMBOL		Value						
STMBOL	Min	Nom	Max					
Α	2.15	2.30	2.45					
A1		1.80 REF						
b	0.70	0.80	0.90					
b1	9.65	9.80	9.95					
b3	1.10	1.20	1.30					
c	0.40	0.50	0.60					
D	10.18	10.38	10.58					
D1	10.98	11.08	11.18					
D2	3.15	3.30	3.45					
D4	4.40	4.55	4.70					
E	9.70	9.90	10.10					
E1	7.95	8.10	8.25					
E2	0.60	0.70	0.80					
e		1.20 BSC						
н	11.48	11.68	11.88					
H1	6.80	6.95	7.10					
i i		0.10 REF						
j1		0.46 REF						
j2		0.20 REF						
К		2.80 REF						
L	1.40	1.90	2.10					
L1	0.50	0.70	0.90					
L2	0.48	0.60	0.72					
L3	0.30	0.70	0.80					
Q		6.80 REF						
R	3.00	3.10	3.20					
θ		10°						

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1:Gate Source Kelvin

3-8 : Source

### **Applications Information**

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance (R<sub>DS(on</sub>)), output capacitance (C<sub>oss</sub>), gate charge (Q<sub>G</sub>), and reverse recovery charge (Q<sub>r</sub>) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see https://www.qorvo.com/design-hub.

A snubber circuit with a small R<sub>(G)</sub>, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high R<sub>(G)</sub> value. There is no extra gate delay time when using the snubber circuitry, and a small  $R_{(G)}$  will better control both the turn-off  $V_{(DS)}$  peak spike and ringing duration, while a high R<sub>(G)</sub> will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high R<sub>(G)</sub>, while greatly reducing E<sub>(OFF)</sub> from mid-to-full load range with only a small increase in E(ON). Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at https://www.qorvo.com/design-hub.



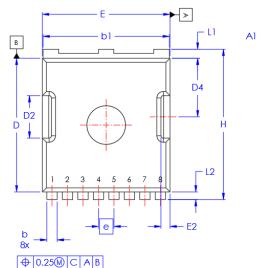


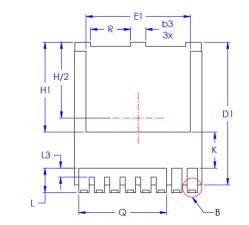
#### Important notice

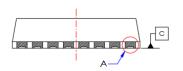
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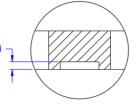


#### PACKAGE OUTLINE

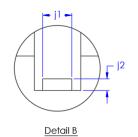








С



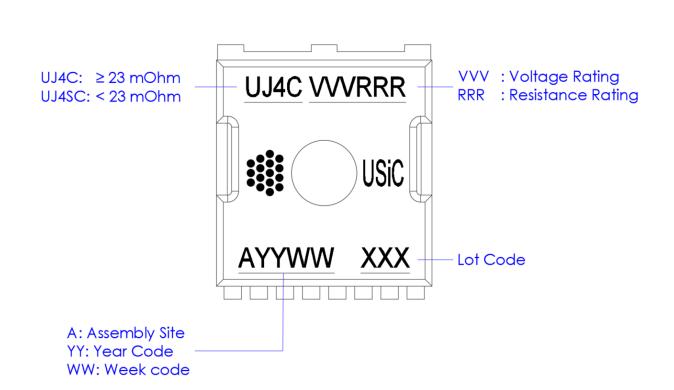
<u>Detail A</u>

- Note: 1. All dimensions in millimeters
  - 2. Dimensions does not include Burrs and Mold Flashes

TO-LL							
SYMBOL	Value						
	Min	Max					
A	2.15	2.45					
Al	1.80	REF					
b	0.65	0.90					
bl	9.65	9.95					
b3	1.10	1.30					
С	0.40	0.60					
D	10.18	10.58					
DI	10.88	11.28					
D2	3.15	3.45					
D4	4.40	4.70					
E	9.70	10.10					
E1	7.95	8.25					
E2	0.60	0.80					
е	1.20	BSC					
Н	11.48	11.88					
H1	6.80	7.10					
i	0.10	REF					
j1	0.46	REF					
j2	0.20	REF					
K	2.80	REF					
L	1.40	2.10					
L1	0.50	0.90					
L2	0.48	0.72					
L3	0.30	0.80					
Q	6.80	REF					
R	3.00	3.20					



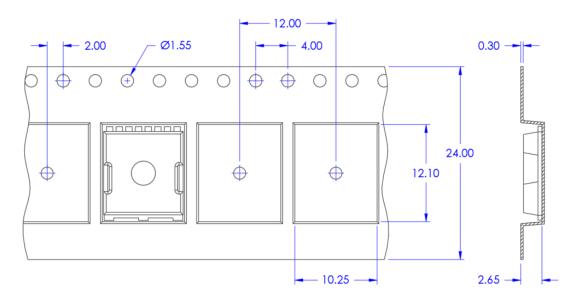
PART MARKING



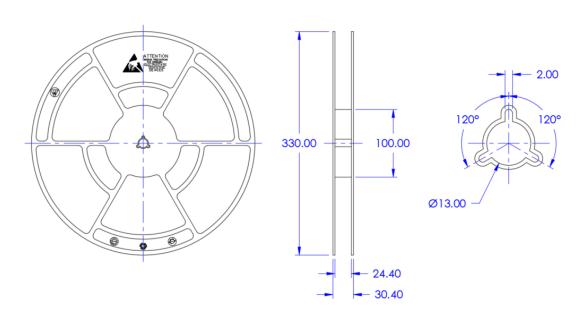


#### PACKING TYPE

#### Carrier Tape



<u>Reel</u>



All dimensions in millimeters Quantity per Reel: 2000 units



TOLL PACKAGE OUTLINE, PART MARKING, TAPE AND REEL SPECIFICATION	Page <b>4</b> of <b>4</b>
DS_TOLL	Rev B

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#### **REVISION HISTORY**

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
А	10/13/2023	Initial Production Release	Glenn Galang
В	01/31/2024	Corrected device orientation inside carrier tape pocket (Page 3)	Glenn Galang

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