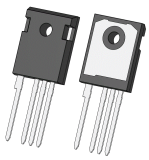
Silicon Carbide (SiC) Combo JFET – EliteSiC, Power N-Channel, TO247-4, 750 V, 5.9 mohm

SiC JFET w/ Si MOSFET

UG4SC075006K4S



TO247-4 15.90x20.96x5.03, 5.44P
CASE 340AN

Description

onsemi's UG4SC075006K4S "Combo-FET" integrates both a 750 V SiC JFET and a Low Voltage Si MOSFET into a single TO247-4 package. This innovative approach allows users to create circuitry that would enable a normally-off switch while leveraging the benefits of a normally-on SiC JFET. These benefits include ultra-low on-resistance ($R_{DS(on)}$) to minimize conduction losses and the exceptional robustness characteristic of a simplified JFET device structure, making it capable of handling the high-energy switching required in circuit protection applications. For switch-mode power conversion application, this device provides separate access to the JFET and MOSFET gates for improved speed control and ease of paralleling multiple devices.

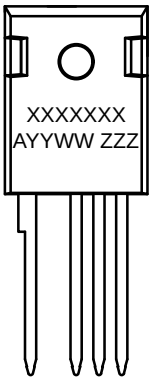
Features

- Single Digit $R_{DS(on)}$
- Normally-off Capability
- Improved Speed Control
- Improved Parallel Device Operation (3+ FETs)
- Operating Temperature: 175 °C (Max)
- High Pulse Current Capability
- Excellent Device Robustness
- Silver-sintered Die Attach for Excellent Thermal Resistance
- Short Circuit Rated
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Typical Applications

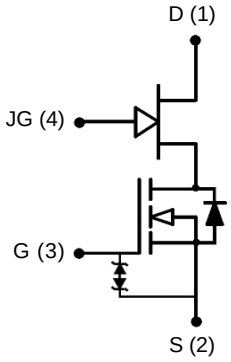
- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- High Power Switch Mode Converters (>25 kW)

MARKING DIAGRAM



XXXXXXXX = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week
ZZZ = Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		750	V
JFET Gate (JG) to Source Voltage	V_{JGS}	DC	−30 to +3	V
		AC (Note 1)	−30 to +30	V
MOSFET Gate (G) to Source Voltage	V_{GS}	DC	−20 to +20	V
		AC (f > 1 Hz)	−25 to +25	V
Continuous Drain Current (Note 2)	I_D	T_C < 125 °C	120	A
Pulsed Drain Current (Note 3)	I_{DM}	T_C = 25 °C	588	A
Single Pulsed Avalanche Energy (Note 4)	E_{AS}	L = 15 mH, I_{AS} = 6.5 A	316	mJ
Short Circuit Withstand Time	t_{SC}	V_{DS} = 400 V, $T_{J(START)}$ = 175 °C	5	μs
SiC FET dv/dt Ruggedness	dv/dt	V_{DS} < 500 V	100	V/ns
Power Dissipation	P_{tot}	T_C = 25 °C	714	W
Maximum Junction Temperature	$T_{J,max}$		175	°C
Operating and Storage Temperature	T_J, T_{STG}		−55 to 175	°C
Max. Lead Temperature for Soldering	T_L		250	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. +30 V ac rating applies for turn-on pulses <200 ns applied with external R_G > 1 Ω.
2. Limited by bondwires
3. Pulse width t_p limited by $T_{J,max}$
4. Starting T_J = 25 °C

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		−	0.16	0.21	°C/W

ELECTRICAL CHARACTERISTICS (T_J = +25 °C and V_{JGS} = 0 V unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
TYPICAL PERFORMANCE − STATIC							
Drain-source Breakdown Voltage	BV_{DS}	V_{GS} = 0 V, V_{JGS} = 0 V, I_D = 1 mA		750	−	−	V
Total Drain Leakage Current	I_{DSS}	V_{DS} = 750 V, V_{GS} = 0 V, V_{JGS} = 0 V, T_J = 25 °C		−	6	130	μA
		V_{DS} = 750 V, V_{GS} = 0 V, V_{JGS} = 0 V, T_J = 175°C		−	45	−	
Total JFET Gate Leakage Current	I_{JGSS}	V_{JGS} = −20 V, V_{GS} = 12 V		−	0.1	100	μA
Total MOSFET Gate Leakage Current	I_{GSS}	V_{GS} = −20 V / +20 V		−	6	20	μA
Drain-source On-resistance	$R_{DS(on)}$	V_{GS} = 12 V, I_D = 80 A	V_{JGS} = 2 V, T_J = 25 °C	−	5.3	−	mΩ
			T_J = 25 °C	−	5.9	7.5	
			T_J = 125 °C	−	9.8	−	
			T_J = 175 °C	−	12.9	−	
JFET Gate Threshold Voltage	$V_{JG(th)}$	V_{DS} = 5 V, V_{GS} = 12 V, I_D = 180 mA		−8.3	−6.0	−3.7	V
MOSFET Gate Threshold Voltage	$V_{G(th)}$	V_{DS} = 5 V, V_{JGS} = 0 V, I_D = 10 mA		4	4.7	6	V
JFET Gate Resistance	R_{JG}	f = 1 MHz, open drain		−	0.8	−	Ω
MOSFET Gate Resistance	R_G	f = 1 MHz, open drain		−	0.8	−	Ω
TYPICAL PERFORMANCE − REVERSE DIODE							
Diode Continuous Forward Current (Note 5)	I_S	T_C < 125 °C		−	−	120	A
Diode Pulse Current (Note 6)	$I_{S,pulse}$	T_C = 25 °C		−	−	588	A

ELECTRICAL CHARACTERISTICS (T_J = +25 °C and V_{JGS} = 0 V unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE − REVERSE DIODE						
Forward Voltage	V_{FSD}	V_{GS} = 0 V, V_{JGS} = 0 V, I_S = 50 A, T_J = 25 °C	−	1.03	1.16	V
		V_{GS} = 0 V, V_{JGS} = 0 V, I_S = 50 A, T_J = 175 °C	−	1.06	−	
Reverse Recovery Charge	Q_{rr}	V_{DS} = 400 V, I_S = 80 A, V_{GS} = 0 V, V_{JGS} = 0 V, R_{JG} = 0.7 Ω, di/dt = 2400 A/μs, T_J = 25 °C	−	377	−	nC
Reverse Recovery Time	t_{rr}		−	70	−	ns
Reverse Recovery Charge	Q_{rr}	V_{DS} = 400 V, I_S = 80 A, V_{GS} = 0 V, V_{JGS} = 0 V, R_{JG} = 0.7 Ω, di/dt = 2400 A/μs, T_J = 150 °C	−	427	−	nC
Reverse Recovery Time	t_{rr}		−	78	−	ns
TYPICAL PERFORMANCE − DYNAMIC WITH MOSFET GATE AS CONTROL TERMINAL AND V_{JGS} = 0 V						
MOSFET Input Capacitance	C_{iss}	V_{DS} = 400 V, V_{GS} = 0 V, f = 100 kHz	−	8374	−	pF
Output Capacitance	C_{oss}		−	362	−	
Reverse Transfer Capacitance	C_{rss}		−	4	−	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	−	475	−	pF
Effective Output Capacitance, Time Related	$C_{oss(tr)}$		−	950	−	pF
C_{OSS} Stored Energy	E_{oss}	V_{DS} = 400 V, V_{GS} = 0 V	−	38	−	μJ
Total Gate Charge	Q_G	V_{DS} = 400 V, I_D = 80 A, V_{GS} = 0 V to 15 V	−	164	−	nC
Gate-drain Charge	Q_{GD}		−	24	−	
Gate-source Charge	Q_{GS}		−	46	−	
Turn-on Delay Time	$t_{d(on)}$	Notes 7 and 8 V_{DS} = 400 V, I_D = 80 A, V_{GS} = 0 V to +15 V, R_{G_ON} = 1 Ω, R_{G_OFF} = 10 Ω, R_{JG_ON} = 0.7 Ω, R_{JG_OFF} = 10 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V, R_G = 10 Ω, R_{JG_ON} = 0.7 Ω, T_J = 25 °C	−	30	−	ns
Rise Time	t_r		−	116	−	
Turn-off Delay Time	$t_{d(off)}$		−	148	−	
Fall Time	t_f		−	120	−	
Turn-on Energy	E_{ON}		−	2185	−	μJ
Turn-off Energy	E_{OFF}		−	1690	−	
Total Switching Energy	E_{TOT}		−	3875	−	
Turn-on Delay Time	$t_{d(on)}$	Notes 7 and 8 V_{DS} = 400 V, I_D = 80 A, V_{GS} = 0 V to +15 V, R_{G_ON} = 1 Ω, R_{G_OFF} = 10 Ω, R_{JG_ON} = 0.7 Ω, R_{JG_OFF} = 10 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V, R_G = 10 Ω, R_{JG_ON} = 0.7 Ω, T_J = 150 °C	−	28	−	ns
Rise Time	t_r		−	124	−	
Turn-off Delay Time	$t_{d(off)}$		−	156	−	
Fall Time	t_f		−	103	−	
Turn-on Energy	E_{ON}		−	2377	−	μJ
Turn-off Energy	E_{OFF}		−	1569	−	
Total Switching Energy	E_{TOT}		−	3946	−	
TYPICAL PERFORMANCE − DYNAMIC WITH JFET GATE AS CONTROL TERMINAL AND V_{GS} = +12 V						
JFET Input Capacitance	C_{Jiss}	V_{DS} = 400 V, V_{JGS} = −20 V, f = 100 kHz	−	3028	−	pF
JFET Output Capacitance	C_{Joss}		−	364	−	
JFET Reverse Transfer Capacitance	C_{Jrss}		−	360	−	
JFET Total Gate Charge	Q_{JG}	V_{DS} = 400 V, I_D = 80 A, V_{JGS} = −18 V to 0 V	−	400	−	nC
JFET Gate-drain Charge	Q_{JGD}		−	270	−	
JFET Gate-source Charge	Q_{JGS}		−	60	−	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Limited by bondwires.
6. Pulse width t_p limited by $T_{J,max}$.
7. Measured with the half-bridge mode switching test circuit in Figure 23.
8. Devices are driven with the ClampDRIVE method as described in the section “Recommended Gate Drive Approach: ClampDRIVE”.

TYPICAL PERFORMANCE DIAGRAMS − MOSFET GATE AS CONTROL TERMINAL AND V_{JGS} = 0 V

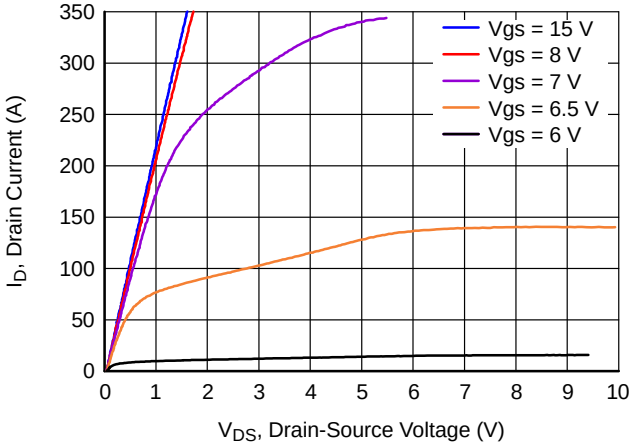


Figure 1. Typical Output Characteristics at T_J = −55 °C, t_p < 250 μs

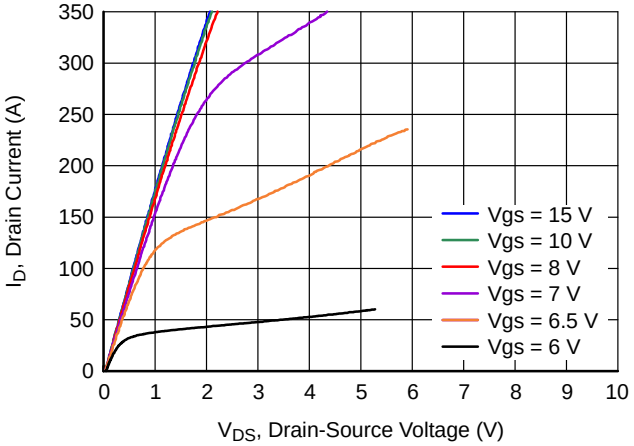


Figure 2. Typical Output Characteristics at T_J = 25 °C, t_p < 250 μs

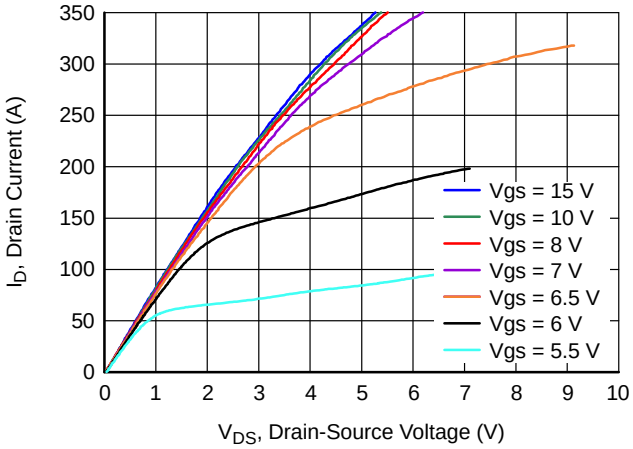


Figure 3. Typical Output Characteristics at T_J = 175 °C, t_p < 250 μs

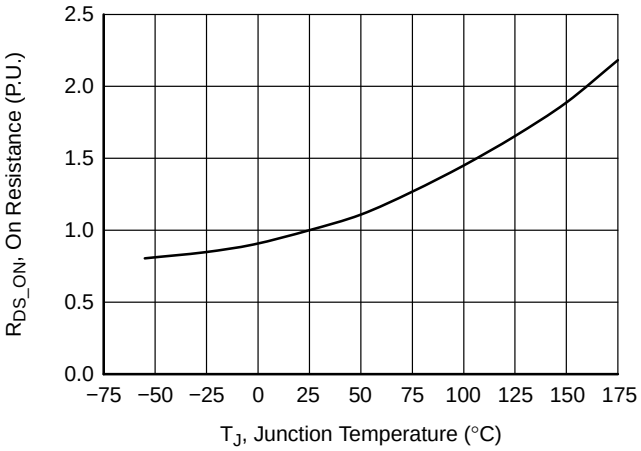


Figure 4. Normalized On-Resistance vs. Temperature at V_{GS} = 12 V and I_D = 80 A

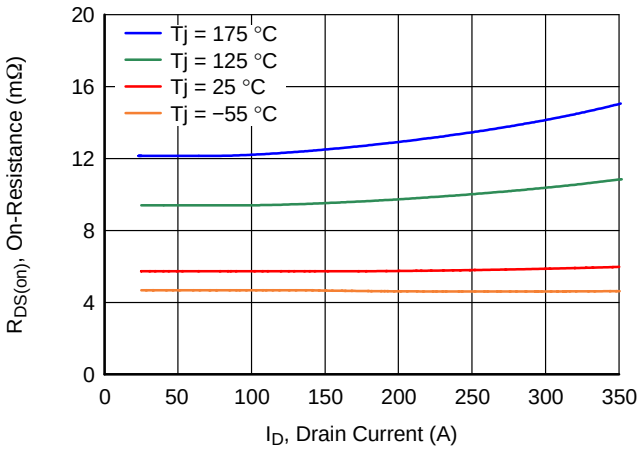


Figure 5. Typical Drain-Source On-Resistances at V_{GS} = 12 V

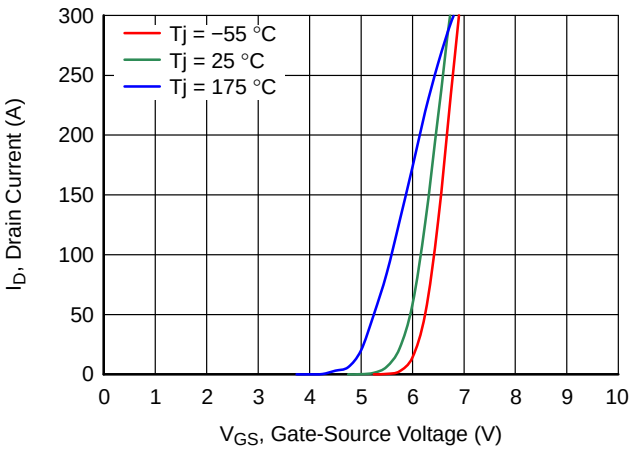


Figure 6. Typical Transfer Characteristics at V_{DS} = 5 V

TYPICAL PERFORMANCE DIAGRAMS − MOSFET GATE AS CONTROL TERMINAL AND V_{JGS} = 0 V

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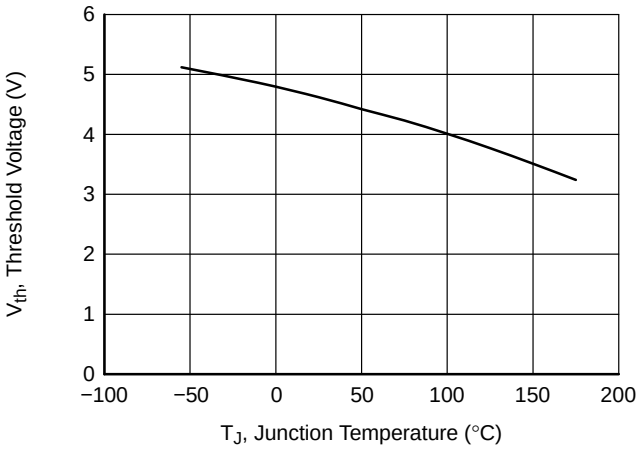

Figure 7. Threshold Voltage vs. Junction Temperature at V_{DS} = 5 V and I_D = 10 mA

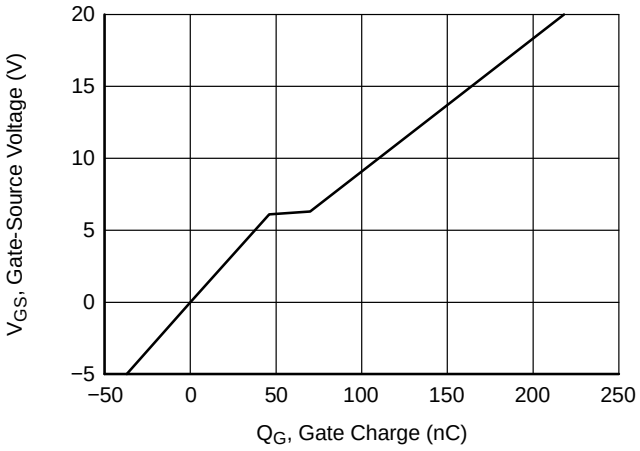

Figure 8. Typical Gate Charge at V_{DS} = 400 V and I_D = 80 A

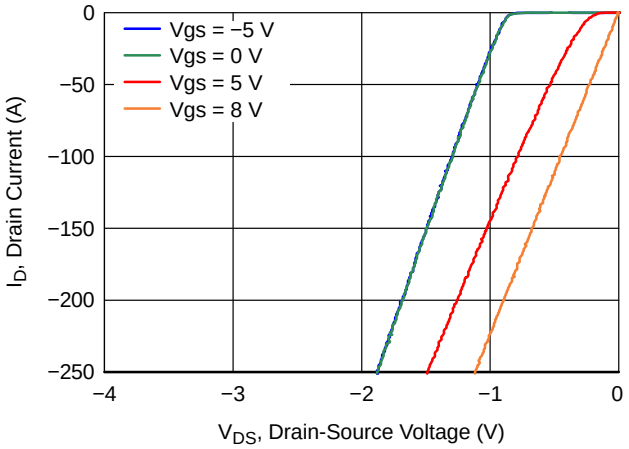

Figure 9. 3rd Quadrant Characteristics at T_J = −55 °C

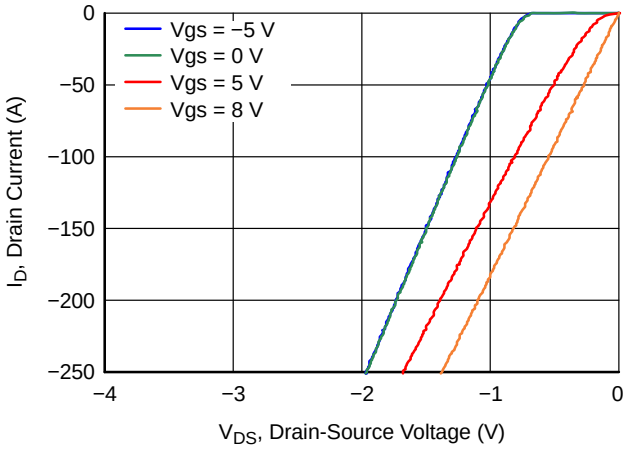

Figure 10. 3rd Quadrant Characteristics at T_J = 25 °C

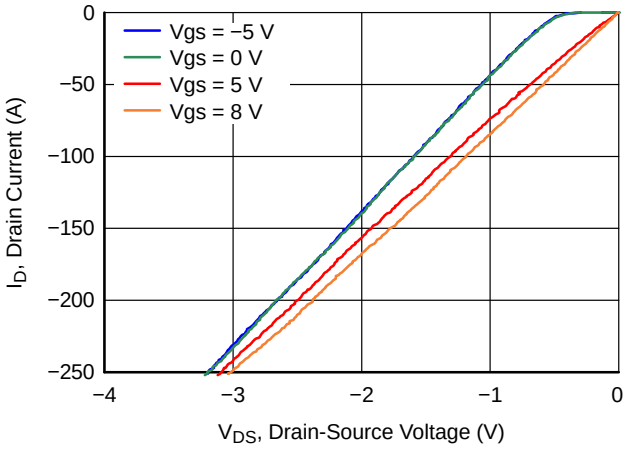

Figure 11. 3rd Quadrant Characteristics at T_J = 175 °C

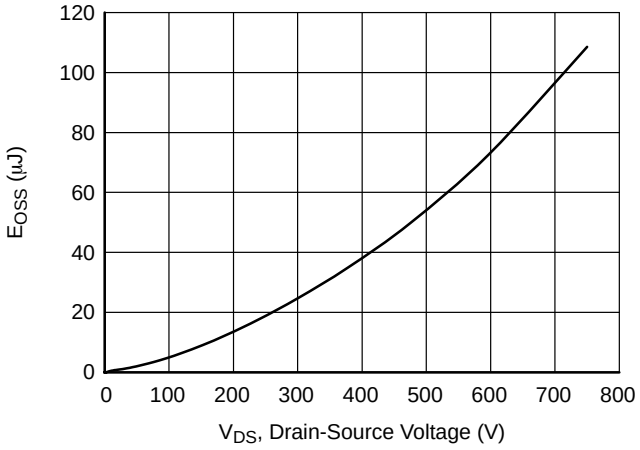

Figure 12. Typical Stored Energy in C_{OSS} at V_{GS} = 0 V

TYPICAL PERFORMANCE DIAGRAMS − MOSFET GATE AS CONTROL TERMINAL AND V_{JGS} = 0 V

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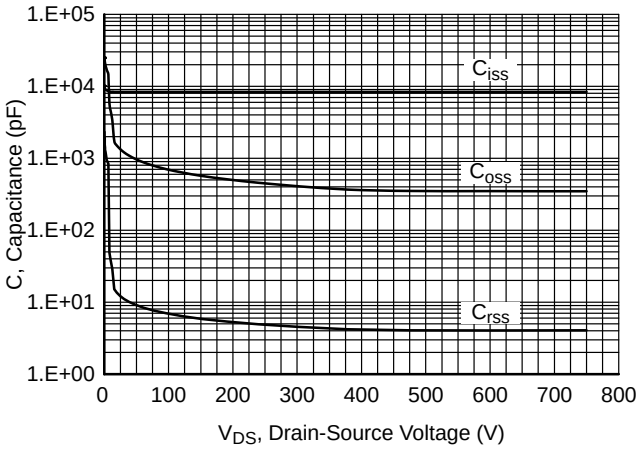

Figure 13. Typical Capacitances at f = 100 kHz and V_{GS} = 0 V

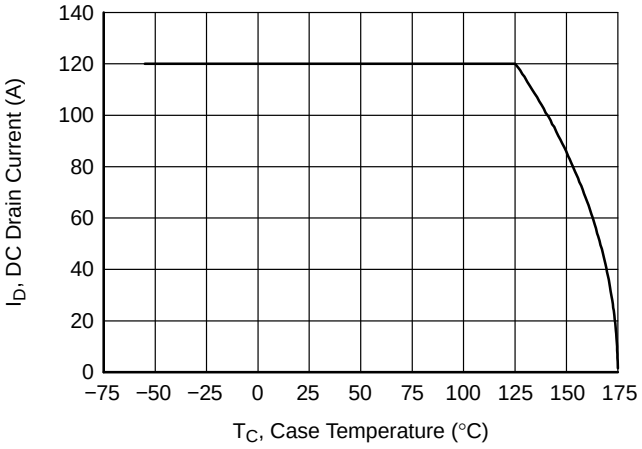

Figure 14. DC Drain Current Derating

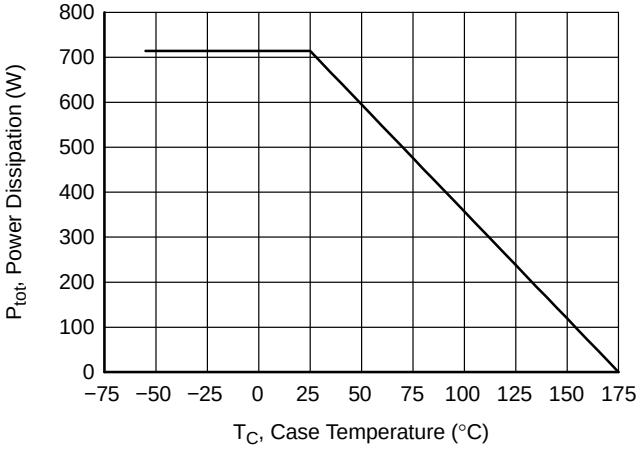

Figure 15. Total Power Dissipation

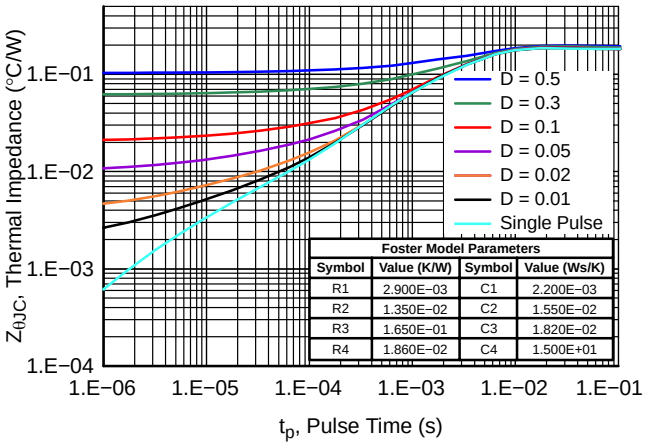

Figure 16. Maximum Transient Thermal Impedance

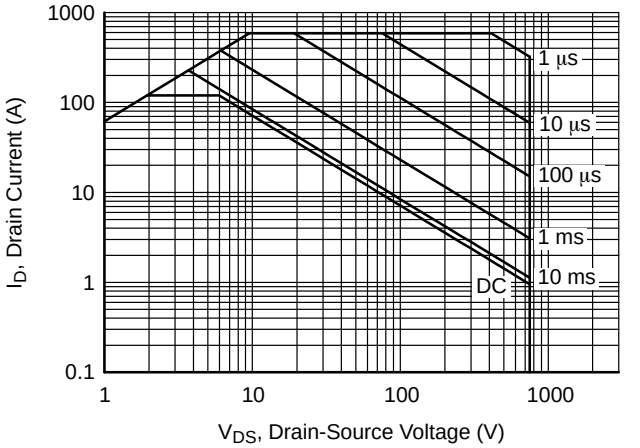

Figure 17. Safe Operation Area at T_C = 25 °C, D = 0, Parameter t_p

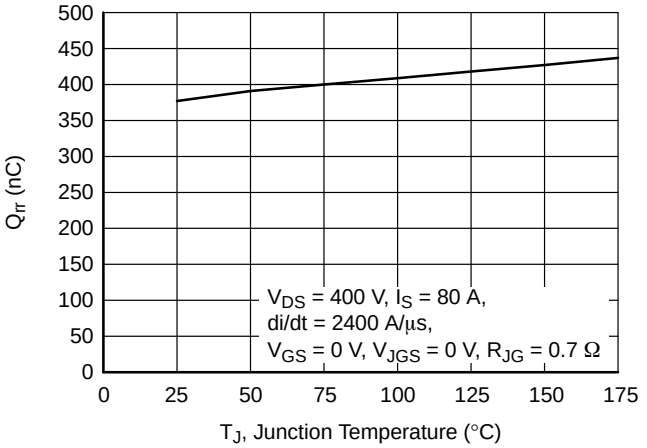

Figure 18. Reverse Recovery Charge Q_{rr} vs. Junction Temperature

TYPICAL PERFORMANCE DIAGRAMS − MOSFET GATE AS CONTROL TERMINAL AND V_{JGS} = 0 V

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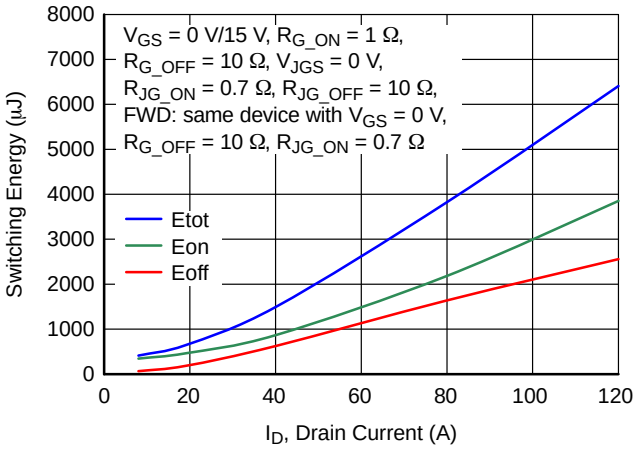


Figure 19. Clamped Inductive Switching Energy vs. Drain Current at V_{DS} = 400 V and T_J = 25 °C

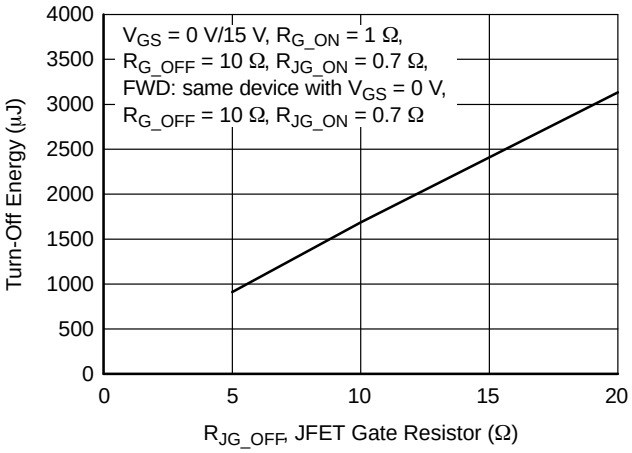


Figure 20. Clamped Inductive Turn-Off Energy vs. JFET Gate Resistor R_{JG_OFF} at V_{DS} = 400 V, I_D = 80 A, and T_J = 25 °C

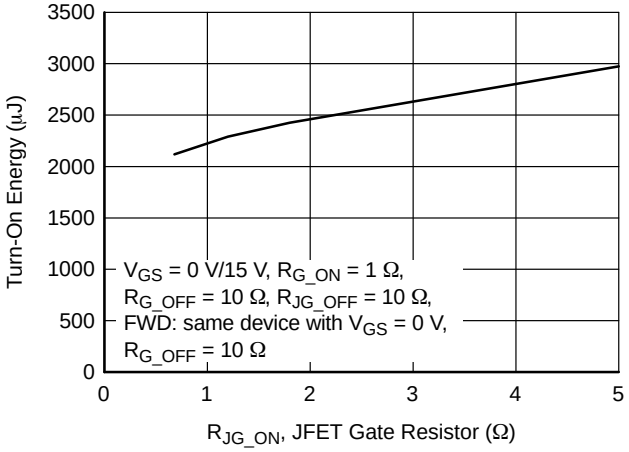


Figure 21. Clamped Inductive Turn-On Energy vs. JFET Gate Resistor R_{JG_ON} at V_{DS} = 400 V, I_D = 80 A, and T_J = 25 °C

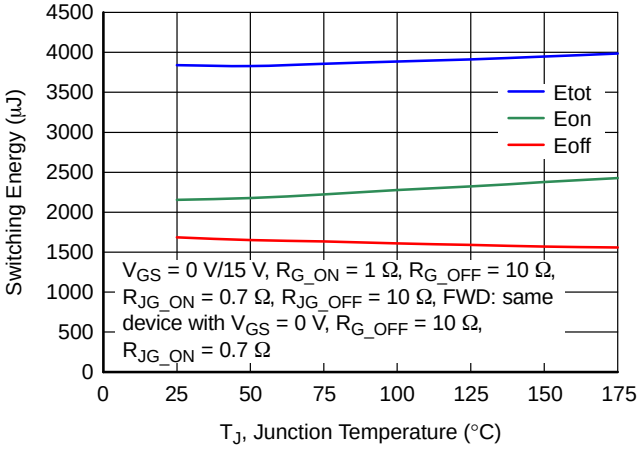


Figure 22. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 400 V and I_D = 80 A

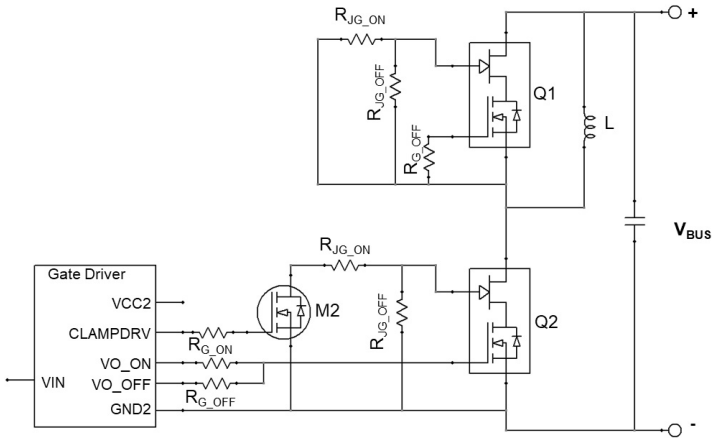


Figure 23. Schematic of the Half-bridge Mode Switching Test Circuit with ClampDRIVE Method

TYPICAL PERFORMANCE DIAGRAMS − JFET GATE AS CONTROL TERMINAL AND V_{GS} = +12 V

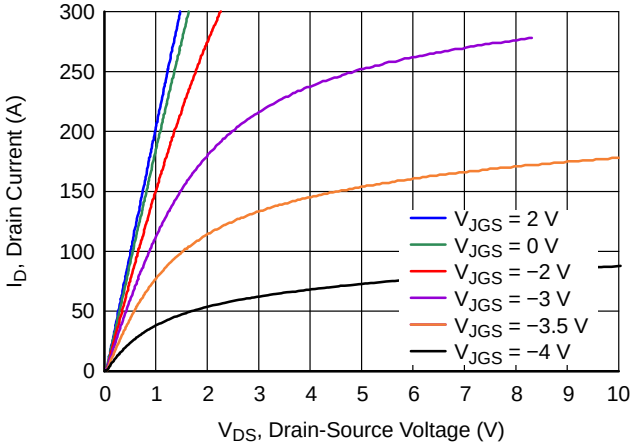


Figure 24. Typical Output Characteristics with JFET Gate as Control at T_J = − 55 °C, t_p < 250 μs

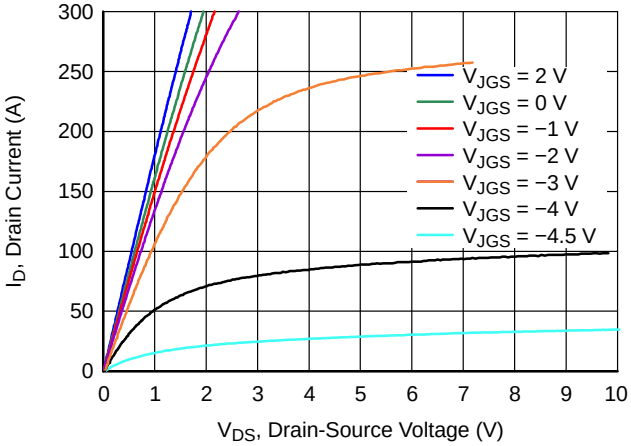


Figure 25. Typical Output Characteristics with JFET Gate as Control at T_J = 25 °C, t_p < 250 μs

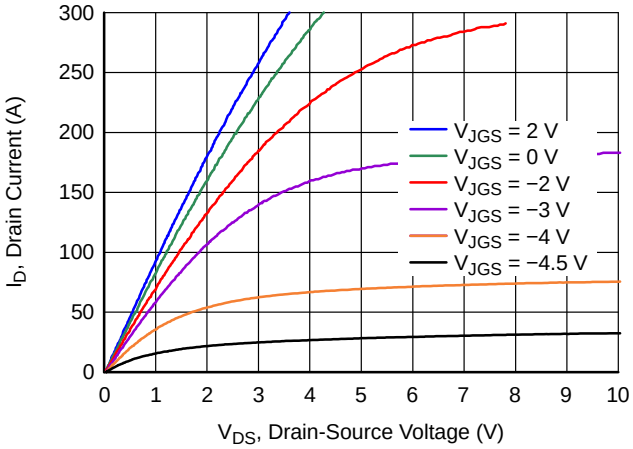


Figure 26. Typical Output Characteristics with JFET Gate as Control at T_J = 175 °C, t_p < 250 μs

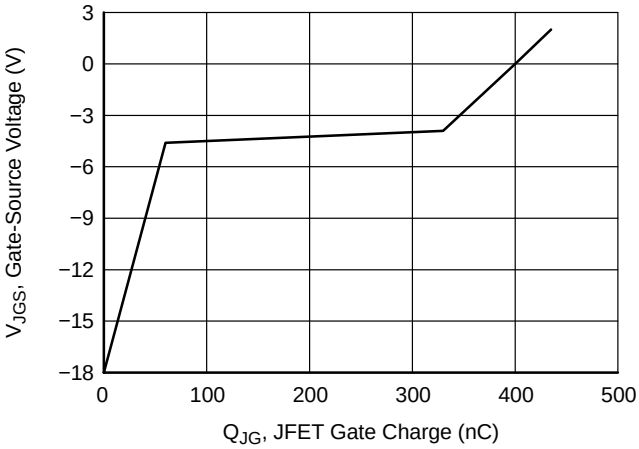


Figure 27. Typical JFET gate charge at V_{DS} = 400 V and I_D = 80 A

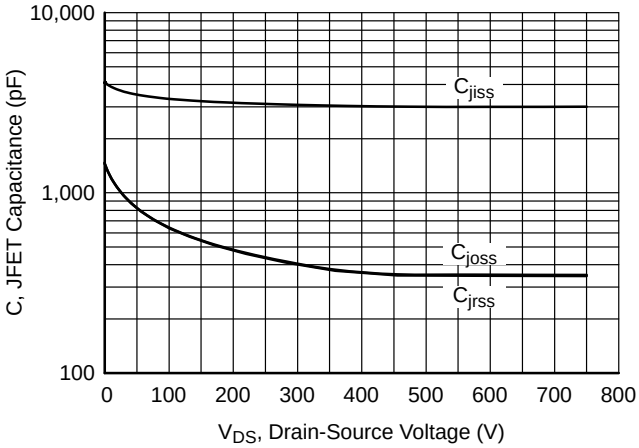


Figure 28. Typical JFET Capacitances at f = 100 kHz and V_{JGS} = −20 V

RECOMMENDED GATE DRIVE APPROACH: CLAMPDRIVE METHOD

Since both JFET gate and MOSFET gate are accessible, more parameters and approaches can be used to control the switching behavior of the device and make the device suitable for a wide range applications from solid state circuit breakers requiring ultra-high current turn-off capability to motor drives requiring well controlled switching speed. The recommended gate drive approach is the ClampDRIVE method, with which the desired turn-on speed, turn-off speed and reverse recovery performance can be achieved at the same time. The main idea of this method is to dynamically tune the JFET gate resistor value R_{JG} such that, in the off-state, R_{JG} is small enough not to cause a reverse recovery issue, and during turn-off transient, R_{JG} is set to a higher value for the desired turn-off performance. This method can be easily implemented using a commercial off-the-shelf gate driver with miller clamp pre-driver output, as illustrated in Figure 29. VIN is the gate driver input signal. VO is the gate driver output and CLAMPDRV is the gate driver miller clamp pre-driver output. M2 is the clamp MOSFET used to control the JFET gate resistance. The MOSFET M2 is directly controlled by the CLAMPDRV signal.

In the on-state, CLAMPDRV is low which turns the MOSFET M2 off, thus, the effective JFET gate resistance is R_{JG_OFF}. During the turn-off transient, CLAMPDRV is kept low until the device is fully off. This means the JFET gate resistance is R_{JG_OFF} during the turn-off process, and R_{GJ_OFF} can be used to effectively control turn-off speed. After the device is fully off, CLAMPDRV is changed to high level, which turns the MOSFET M2 on.

In the off-state, CLAMPDRV is high and the clamp MOSFET M2 is in on-state. The effective JFET gate resistance is equal to the parallel combination of R_{JG_OFF} and R_{JG_ON}. R_{JG_ON} can be selected small enough to prevent the reverse recovery issue. During the turn-on transient, the JFET gate current may flow from the cascode source through the body diode of the MOSFET M2 and R_{JG_ON} into the JFET gate, so, the turn-on process is also determined by R_{JG_ON}.

In summary, the optimum switching performance of the SiC cascode FETs can be realized with the ClampDRIVE method by selecting proper JFET gate resistors R_{JG_ON} and R_{JG_OFF}.

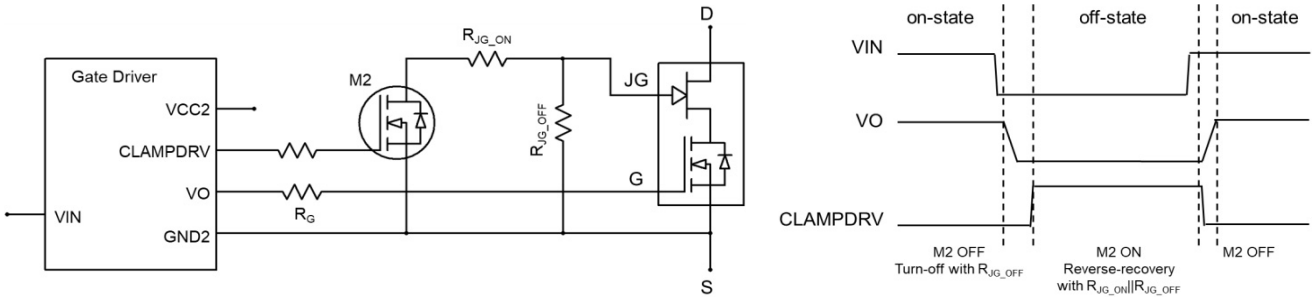
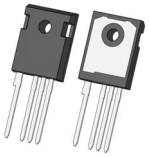


Figure 29. Circuit Schematic and Timing Diagram of the ClampDRIVE Method

ORDERING INFORMATION

Part Number	Marking	Package	Shipping†
UG4SC075006K4S	UG4SC075006K4S	TO247-4 15.90x20.96x5.03, 5.44P (Pb-Free, Halogen Free)	600 / Tube



TO247−4 15.90x20.96x5.03, 5.44P
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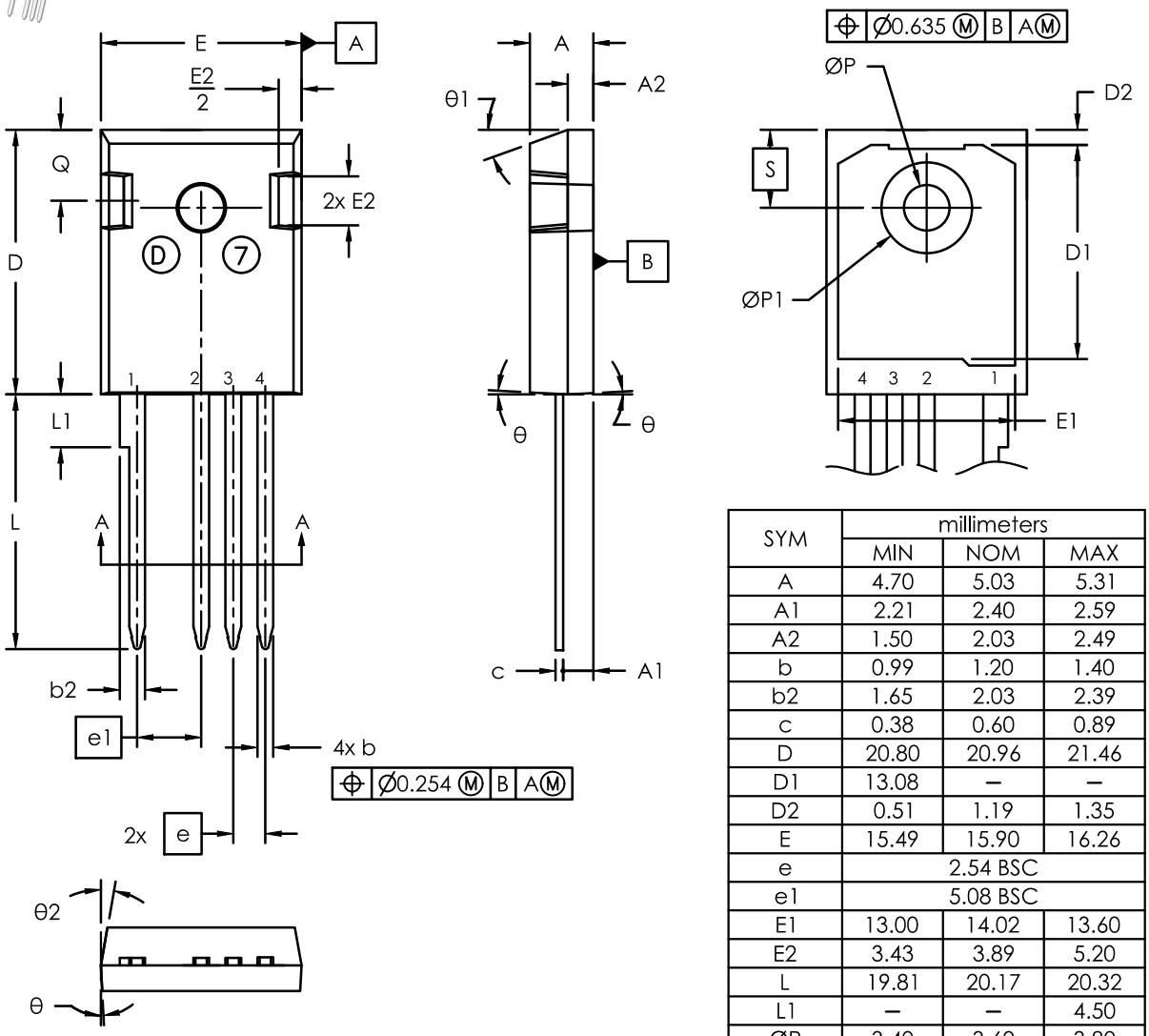

SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
c	0.38	0.60	0.89
D	20.80	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	2.54 BSC		
e1	5.08 BSC		
E1	13.00	14.02	13.60
E2	3.43	3.89	5.20
L	19.81	20.17	20.32
L1	—	—	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.17 BSC		
θ	3°		
θ1	20°		
θ2	10°		

NOTE:
1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.
5. Through Hole diameter value = End Hole diameter
6. PCB Through Hole pattern as per IPC-2221/IPC-2222

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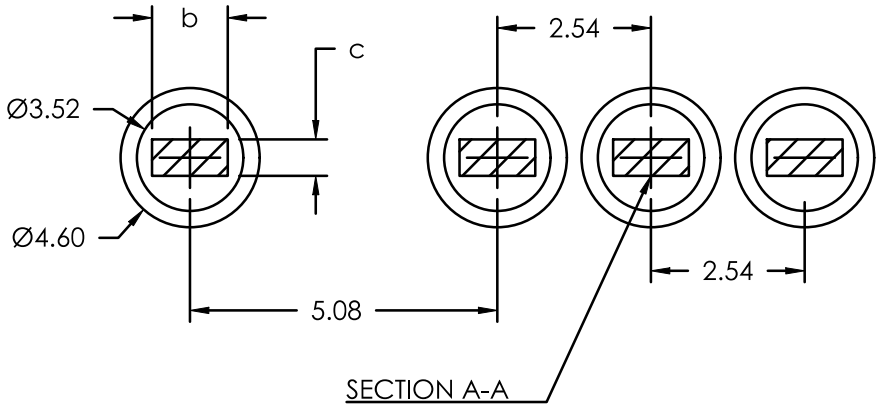
RECOMMENDED PCB THROUGH HOLE



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

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