SiC JFET Division

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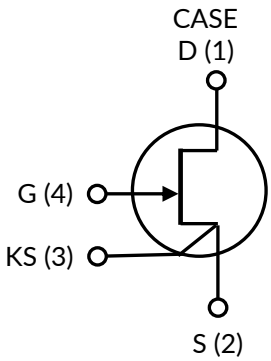
DATASHEET

UF3N120007K4S

Silicon Carbide (SiC) JFET - EliteSiC, Power N-Channel, TO-247-4L, 1200 V, 7.1 mohm

Rev. D, January 2025



Part Number	Package	Marking
UF3N120007K4S	TO-247-4L	UF3N120007K4S

Description

Qorvo's UF3N120007K4S is a 1200 V, 7.1mΩ high-performance Gen 3 normally-on SiC JFET transistor. This device exhibits ultra-low on resistance ($R_{DS(on)}$) in a TO-247-4L package, making it an ideal fit to address the challenging thermal constraints of solid-state circuit breakers and relay applications. Additionally, the JFET is a robust device technology capable of the high-energy switching required in circuit protection applications.

Features

- Single digit on-resistance
- Operating temperature: 175°C (max)
- High pulse current capability
- Excellent device robustness
- Silver-sintered die attach for excellent thermal resistance
- RoHS compliant
- AECQ Qualified

Typical applications

- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-30 to +3	V
		AC [1]	-30 to +30	V
Continuous drain current [2]	I_D	T_C < 112°C	120	A
Pulsed drain current [3]	I_{DM}	T_C = 25°C	550	A
Power dissipation	P_{tot}	T_C = 25°C	789	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J,T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	°C

1. +30V AC rating applies for turn-on pulses <200ns applied with external R_G > 1Ω.
2. Limited by bondwires
3. Pulse width t_p limited by $T_{J,max}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.15	0.19	°C/W

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=-20V, I_D=1mA	1200			V
Total drain leakage current	I_{DSS}	V_{DS}=1200V, V_{GS}=-20V, T_J=25°C		20	300	µA
		V_{DS}=1200V, V_{GS}=-20V, T_J=175°C		100		
Total gate leakage current	I_{GSS}	V_{GS}=-20V, T_J=25°C		15	300	µA
		V_{GS}=-20V, T_J=175°C		55		µA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=2V, I_D=100A, T_J=25°C		7.1		mΩ
		V_{GS}=0V, I_D=100A, T_J=25°C		8.6	11	
		V_{GS}=2V, I_D=100A, T_J=175°C		15.5		
		V_{GS}=0V, I_D=100A, T_J=175°C		17.8		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=320mA	-9.3	-7	-4.7	V
Gate resistance	R_G	f=1MHz, open drain		0.54		Ω

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=800V, V_{GS}=-20V f=100kHz		8110		pF
Output capacitance	C_{oss}			368		
Reverse transfer capacitance	C_{rss}			358		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 800V, V_{GS}=-20V		403		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=800V, V_{GS}=-20V		130		µJ
Total gate charge	Q_G	V_{DS}=800V, I_D=100A, V_{GS} = -18V to 0V		830		nC
Gate-drain charge	Q_{GD}			520		
Gate-source charge	Q_{GS}			120		

Typical Performance Diagrams

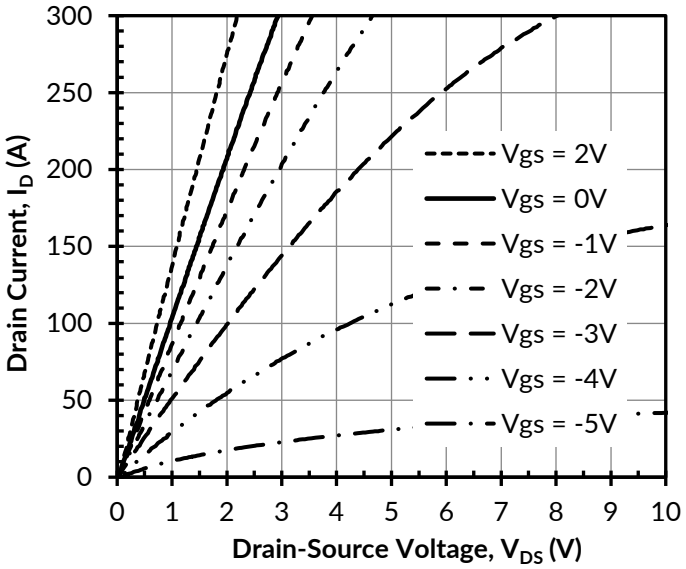


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250µs

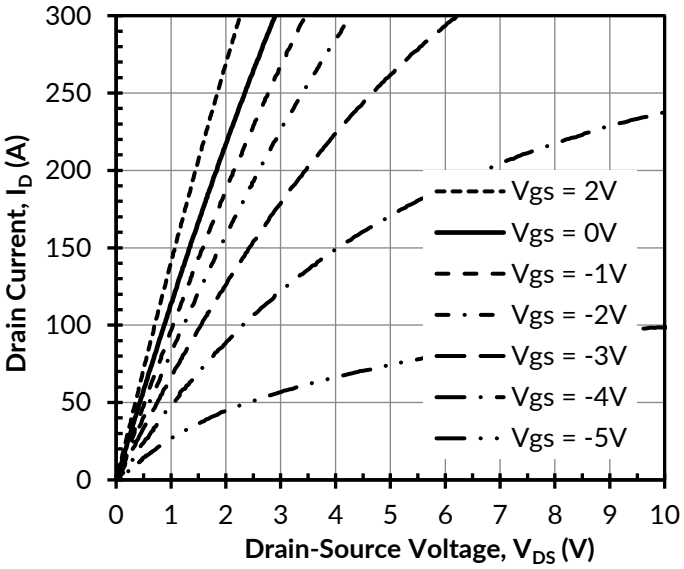


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

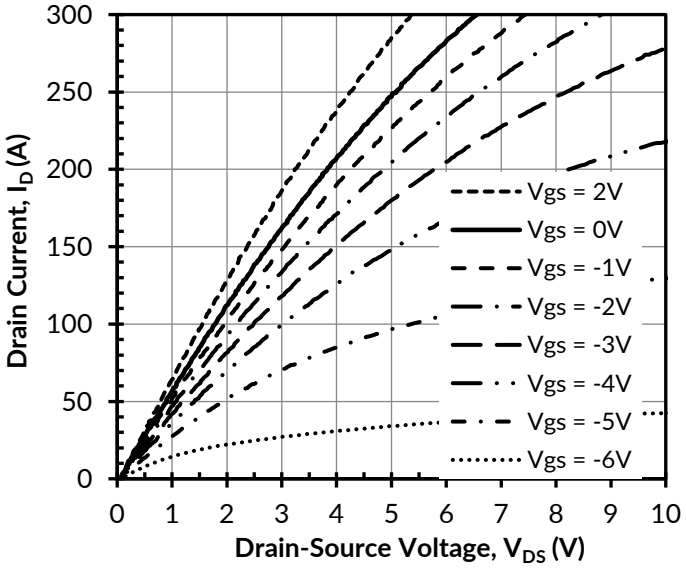


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250µs

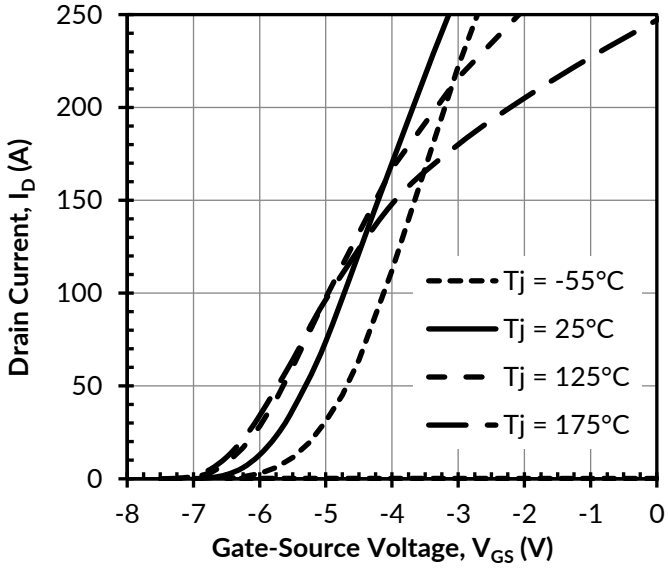


Figure 4. Typical transfer characteristics at V_{DS} = 5V

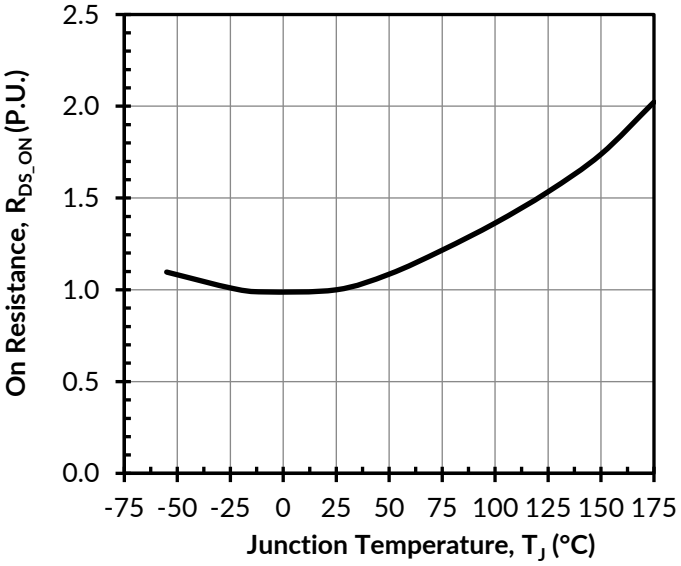


Figure 5. Normalized on-resistance vs. temperature at V_{GS} = 0V and I_D = 100A

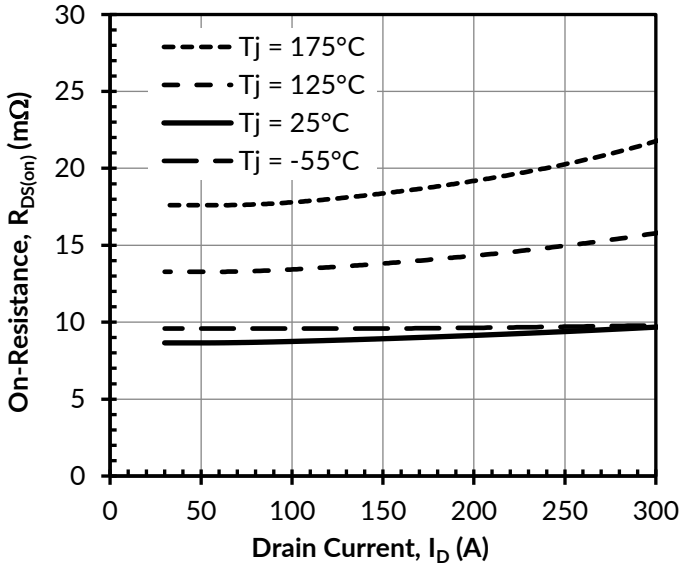


Figure 6. Typical drain-source on-resistances at V_{GS} = 0V

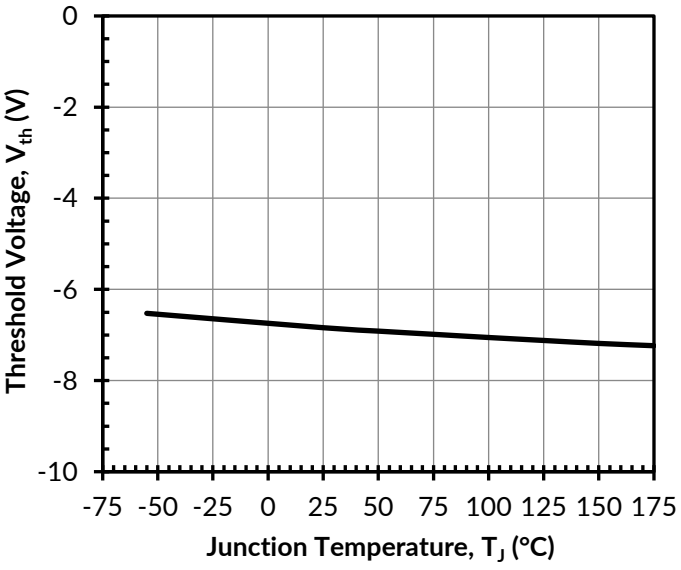


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 320mA

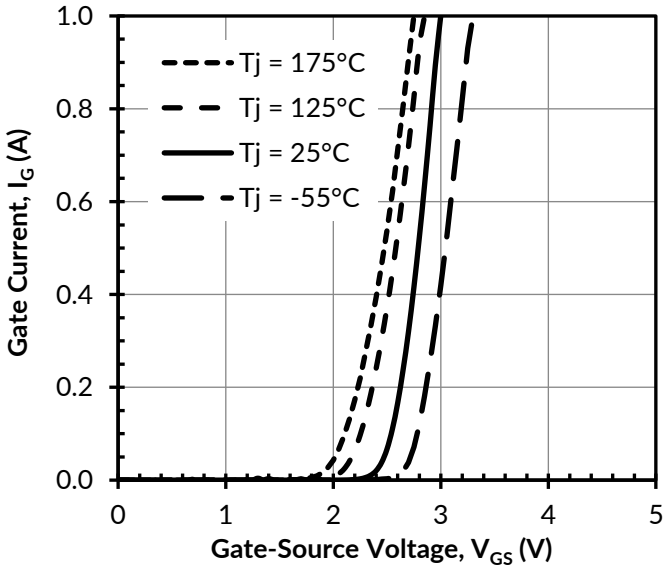


Figure 8. Typical gate forward current at V_{DS} = 0V

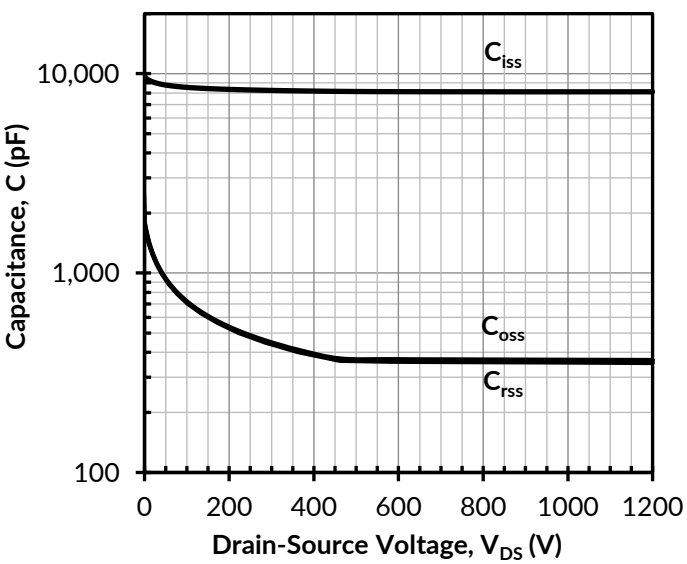


Figure 9. Typical capacitances at f = 100kHz and V_{GS} = -20V

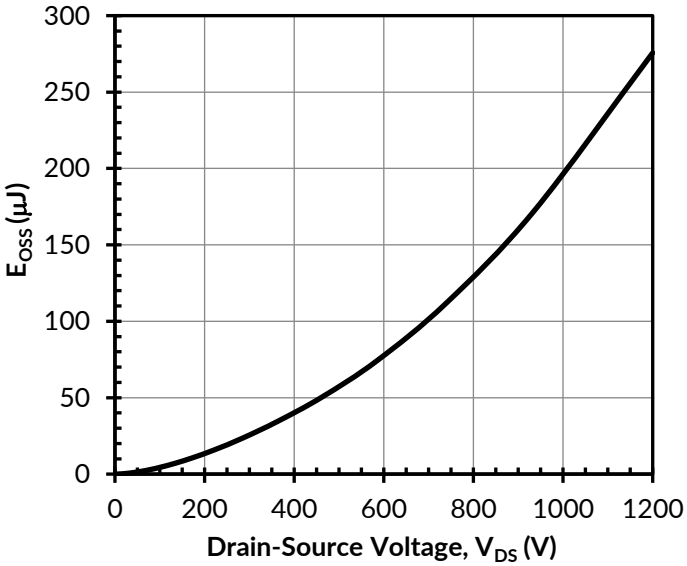


Figure 10. Typical stored energy in C_{OSS} at V_{GS} = -20V

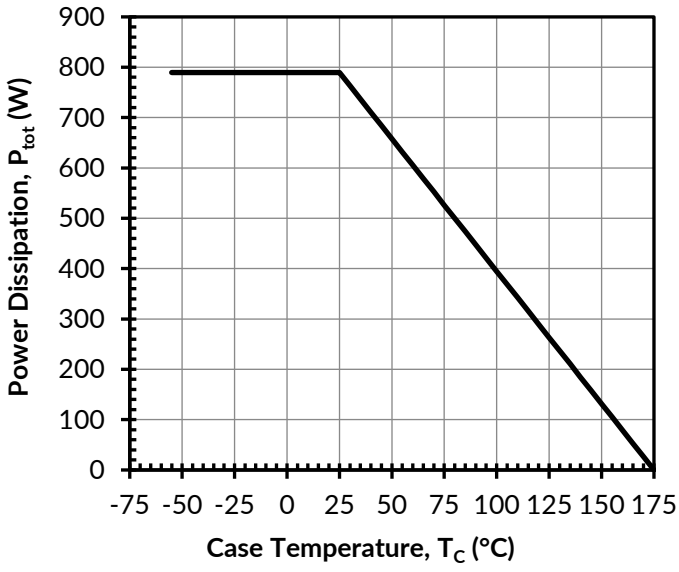


Figure 11. Total power Dissipation

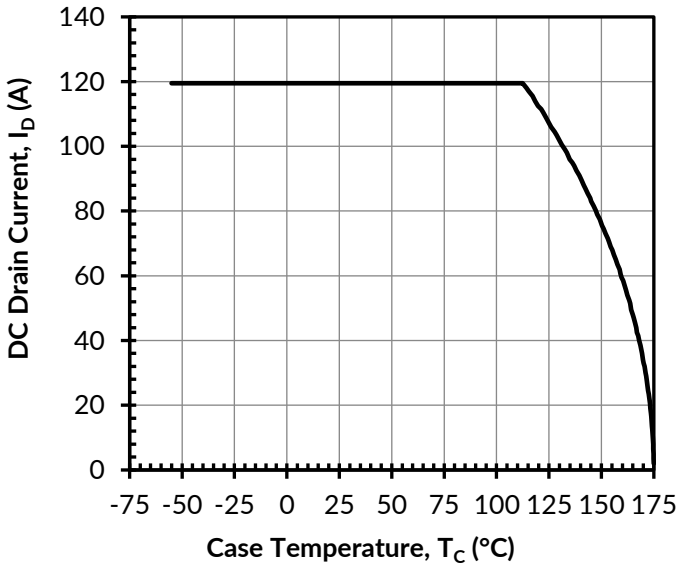


Figure 12. DC drain current derating

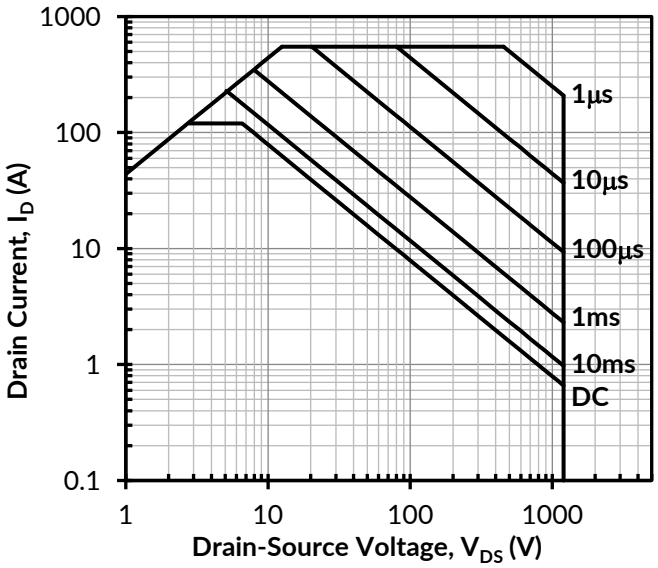


Figure 13. Safe operation area at T_C =25°C, Parameter t_p

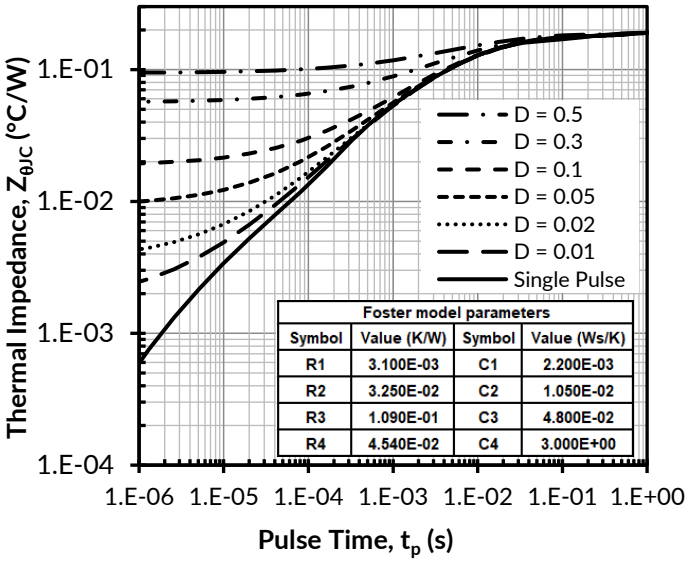


Figure 14. Maximum transient thermal impedance

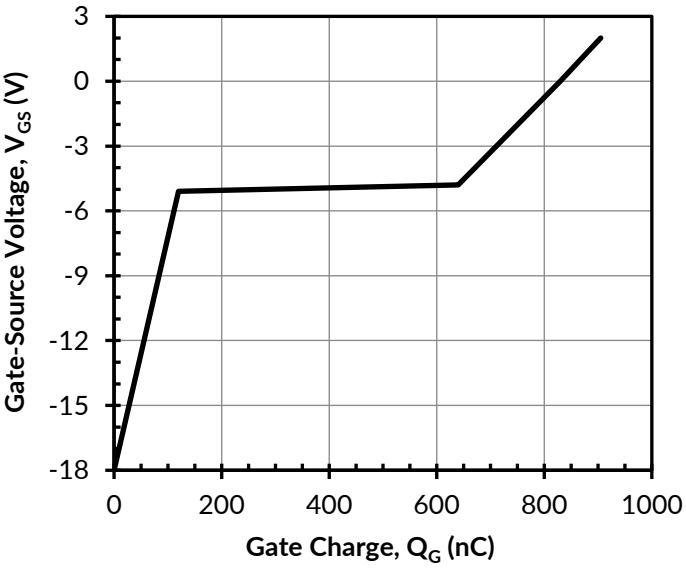


Figure 15. Typical gate charge at V_{DS} = 800V and I_D = 100A

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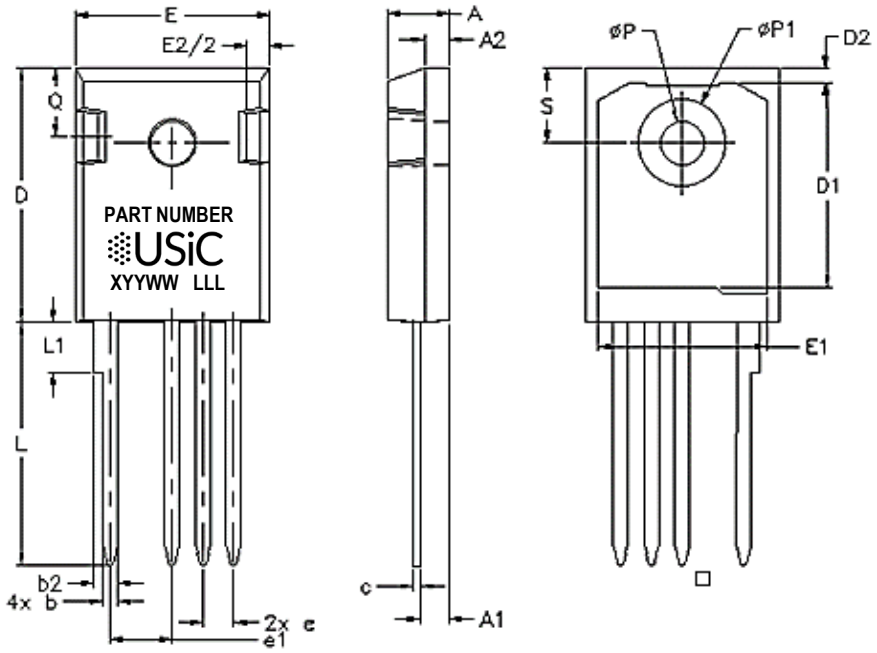
TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

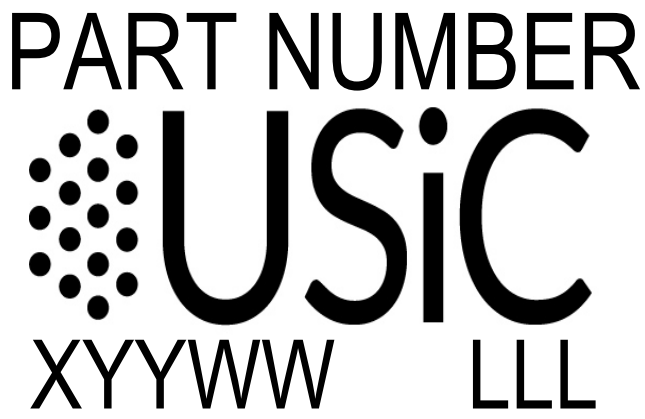
PACKAGE OUTLINE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.185	0.209	4.7	5.31
A1	0.087	0.102	2.21	2.59
A2	0.059	0.098	1.5	2.49
b	0.039	0.055	0.99	1.4
b2	0.065	0.094	1.65	2.39
c	0.015	0.035	0.38	0.89
D	0.819	0.845	20.8	21.46
D1	0.515	-	13.08	-
D2	0.02	0.053	0.51	1.35
E	0.61	0.64	15.49	16.26
e	0.100 BSC		2.54 BSC	
e1	0.19	0.21	4.83	5.33
E1	0.53	-	13.46	-
E2	0.14	0.16	3.56	4.06
L	0.78	0.8	19.81	20.32
L1	-	0.177	-	4.5
ΦP	0.14	0.144	3.56	3.66
ΦP1	0.278	0.291	7.06	7.39
Q	0.212	0.244	5.38	6.2
S	0.243 BSC		6.17 BSC	

TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PART MARKING



PART NUMBER = REFER TO DS_PN DECODER FOR DETAILS

X = ASSEMBLY SITE
YY = YEAR
WW = WORK WEEK
LLL = LOT ID

PACKING TYPE

ANTI-STATIC TUBE

QUANTITY /TUBE : 30 UNITS

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