

QORVO

SiC JFET Division

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DATASHEET

UF3C120150B7S

Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, D²PAK-7L, 1200 V, 150 mohm

Rev. C, Jan 2025

Description

This SiC FET device is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D²PAK-7L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive.

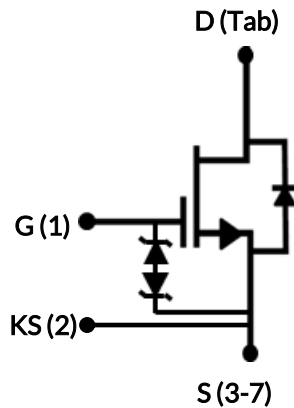
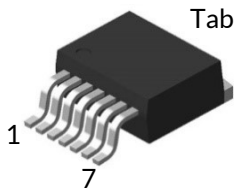
Features

- ◆ On-resistance $R_{DS(on)}$: 150m Ω (typ)
- ◆ Operating temperature: 175°C (max)
- ◆ Excellent reverse recovery: Q_{rr} = 67nC
- ◆ Low body diode V_{FSD} : 1.46V
- ◆ Low gate charge: Q_G = 25.7nC
- ◆ Threshold voltage $V_{G(th)}$: 4.4V (typ) allowing 0 to 15V drive
- ◆ Package creepage and clearance distance > 6.1mm
- ◆ Kelvin source pin for optimized switching performance
- ◆ ESD protected, HBM class 2

Typical applications

Any controlled environment such as

- ◆ Telecom and Server Power
- ◆ Industrial power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating



Part Number	Package	Marking
UF3C120150B7S	D ² PAK-7L	UF3C120150B7S



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current ¹	I_D	$T_C = 25^\circ\text{C}$	17	A
		$T_C = 100^\circ\text{C}$	12.5	A
Pulsed drain current ²	I_{DM}	$T_C = 25^\circ\text{C}$	38	A
Single pulsed avalanche energy ³	E_{AS}	$L=15\text{mH}, I_{AS}=2\text{A}$	30	mJ
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	136	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Reflow soldering temperature	T_{solder}	reflow MSL 3	245	$^\circ\text{C}$

1. Limited by $T_{J,max}$

2. Pulse width t_p limited by $T_{J,max}$

3. Starting $T_J = 25^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.85	1.1	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0V, I_D=1mA$	1200			V
Total drain leakage current	I_{DSS}	$V_{DS}=1200V, V_{GS}=0V, T_J=25^\circ\text{C}$		2	50	μA
		$V_{DS}=1200V, V_{GS}=0V, T_J=175^\circ\text{C}$		17		
Total gate leakage current	I_{GSS}	$V_{DS}=0V, T_J=25^\circ\text{C}, V_{GS}=-20V / +20V$		4	± 20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=5A, T_J=25^\circ\text{C}$		150	180	m Ω
		$V_{GS}=12V, I_D=5A, T_J=125^\circ\text{C}$		250		
		$V_{GS}=12V, I_D=5A, T_J=175^\circ\text{C}$		330		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	3.5	4.4	5.5	V
Gate resistance	R_G	$f=1\text{MHz}, \text{open drain}$		4.6		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C=25^\circ\text{C}$			17	A
Diode pulse current ²	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			38	A
Forward voltage	V_{FSD}	$V_{GS}=0V, I_S=5A, T_J=25^\circ\text{C}$		1.46	2	V
		$V_{GS}=0V, I_S=5A, T_J=175^\circ\text{C}$		2		
Reverse recovery charge	Q_{rr}	$V_R=800V, I_S=13A, V_{GS}=-5V, R_{G,EXT}=22\Omega, di/dt=1700A/\mu\text{s}, T_J=25^\circ\text{C}$		67		nC
Reverse recovery time	t_{rr}	$T_J=25^\circ\text{C}$		24		ns
Reverse recovery charge	Q_{rr}	$V_R=800V, I_S=13A, V_{GS}=-5V, R_{G,EXT}=22\Omega, di/dt=1700A/\mu\text{s}, T_J=150^\circ\text{C}$		64		nC
Reverse recovery time	t_{rr}	$T_J=150^\circ\text{C}$		24		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=100V, V_{GS}=0V$ $f=100kHz$		738		pF
Output capacitance	C_{oss}			58		
Reverse transfer capacitance	C_{rss}			1.8		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 800V, $V_{GS}=0V$		34		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 800V, $V_{GS}=0V$		68		pF
C_{oss} stored energy	E_{oss}	$V_{DS}=800V, V_{GS}=0V$		10.8		μJ
Total gate charge	Q_G	$V_{DS}=800V, I_D=13A,$ $V_{GS} = -5V$ to 12V		25.7		nC
Gate-drain charge	Q_{GD}			6		
Gate-source charge	Q_{GS}			10		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=800V, I_D=13A, \text{Gate Driver} = -5V$ to +12V, Turn-on $R_{G,EXT}=8.5\Omega,$ Turn-off $R_{G,EXT}=20\Omega$ Inductive Load,		32		ns
Rise time	t_r			6		
Turn-off delay time	$t_{d(off)}$			32		
Fall time	t_f			8		
Turn-on energy	E_{ON}	FWD: same device with $V_{GS}=-5V, R_G=20\Omega,$ $T_J=25^\circ C$		208		μJ
Turn-off energy	E_{OFF}			28		
Total switching energy	E_{TOTAL}			236		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=800V, I_D=13A, \text{Gate Driver} = -5V$ to +12V, Turn-on $R_{G,EXT}=8.5\Omega,$ Turn-off $R_{G,EXT}=20\Omega$ Inductive Load,		32		ns
Rise time	t_r			5		
Turn-off delay time	$t_{d(off)}$			32		
Fall time	t_f			7		
Turn-on energy	E_{ON}	FWD: same device with $V_{GS}=-5V, R_G=20\Omega,$ $T_J=150^\circ C$		201		μJ
Turn-off energy	E_{OFF}			23		
Total switching energy	E_{TOTAL}			224		

Typical Performance Diagrams

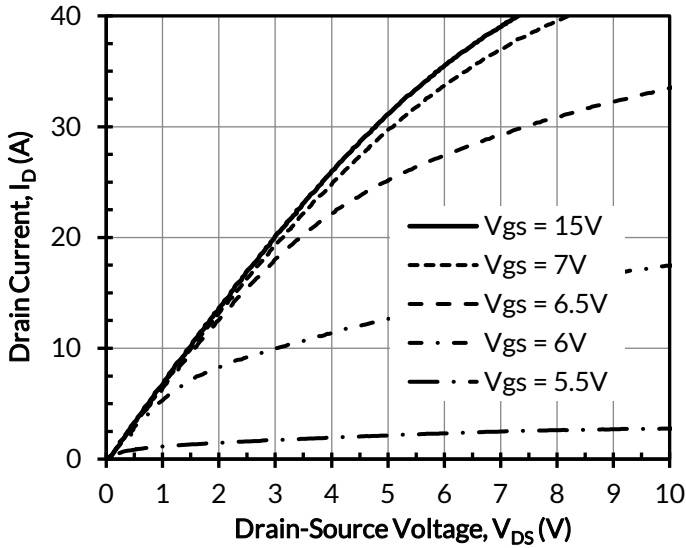


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

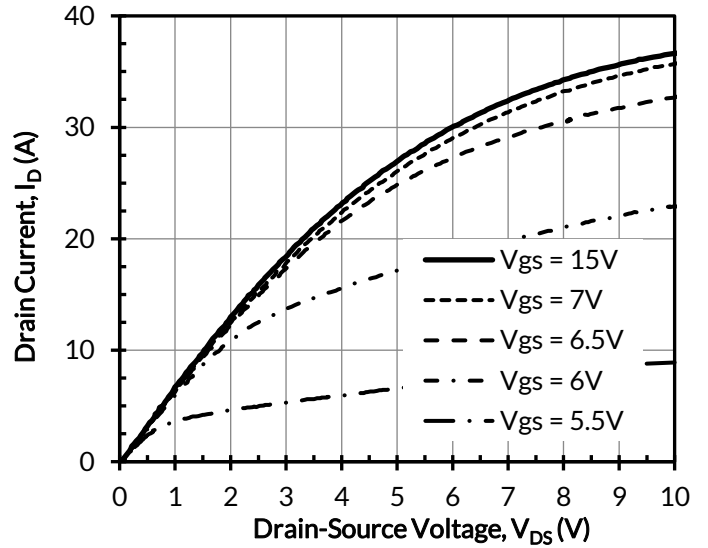


Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

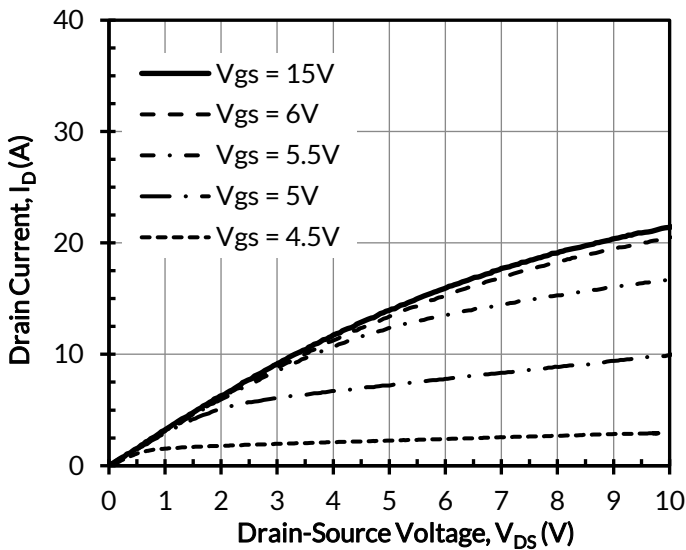


Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

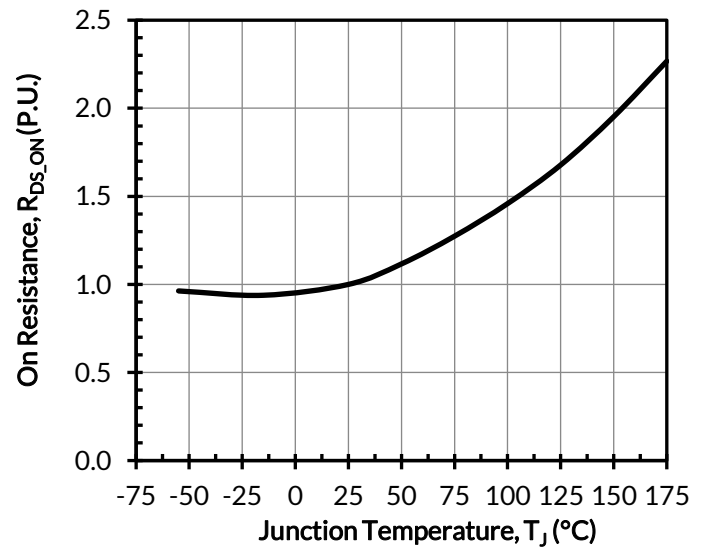


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 5\text{A}$

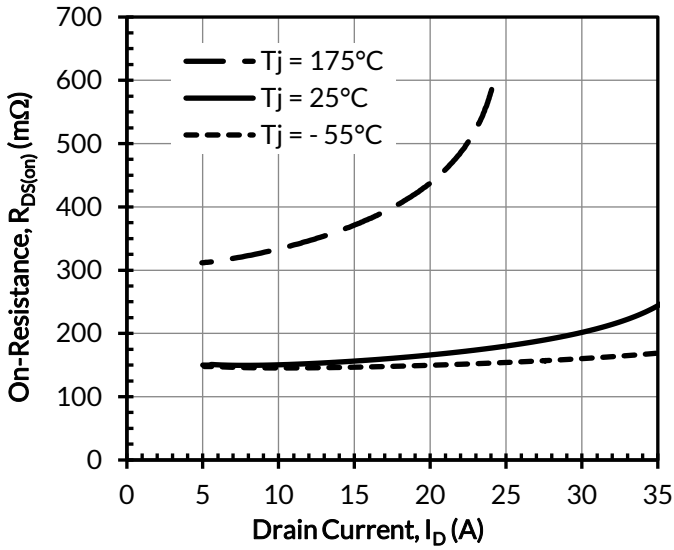


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12\text{V}$

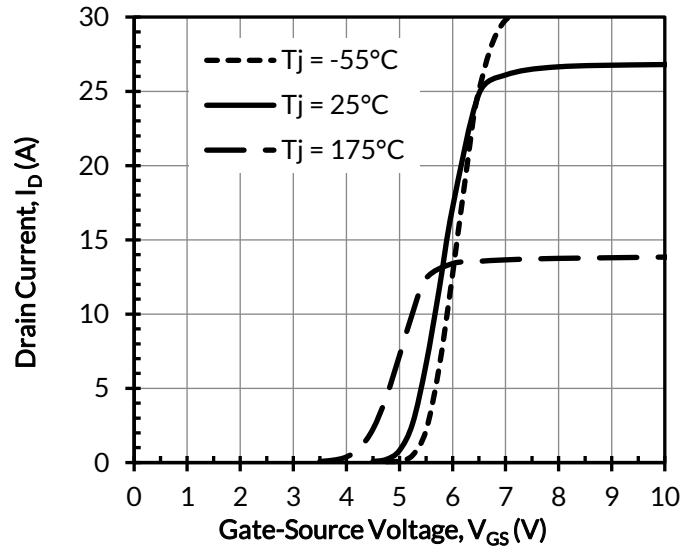


Figure 6. Typical transfer characteristics at $V_{DS} = 5\text{V}$

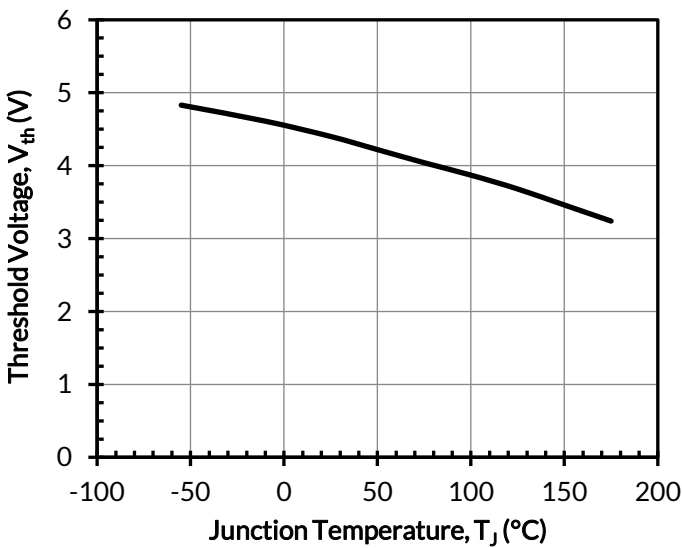


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5\text{V}$ and $I_D = 10\text{mA}$

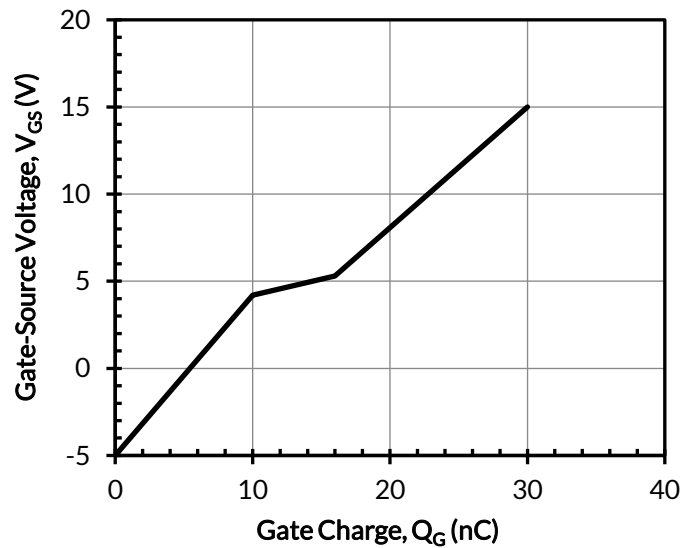


Figure 8. Typical gate charge at $V_{DS} = 800\text{V}$ and $I_D = 13\text{A}$

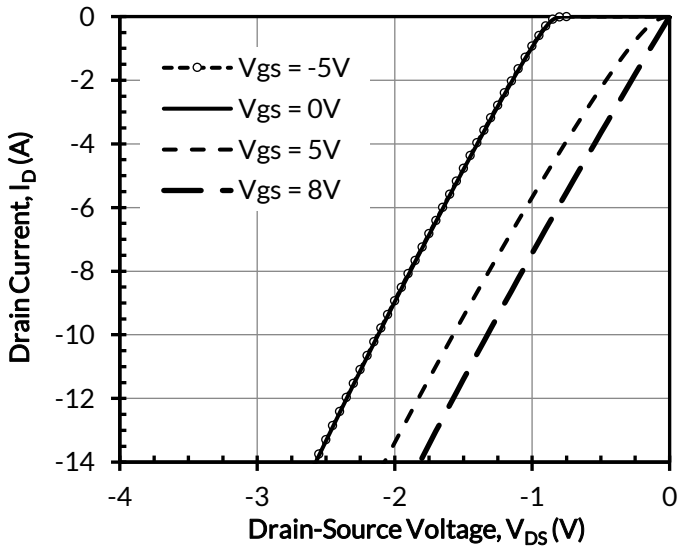


Figure 9. 3rd quadrant characteristics at $T_j = -55^\circ\text{C}$

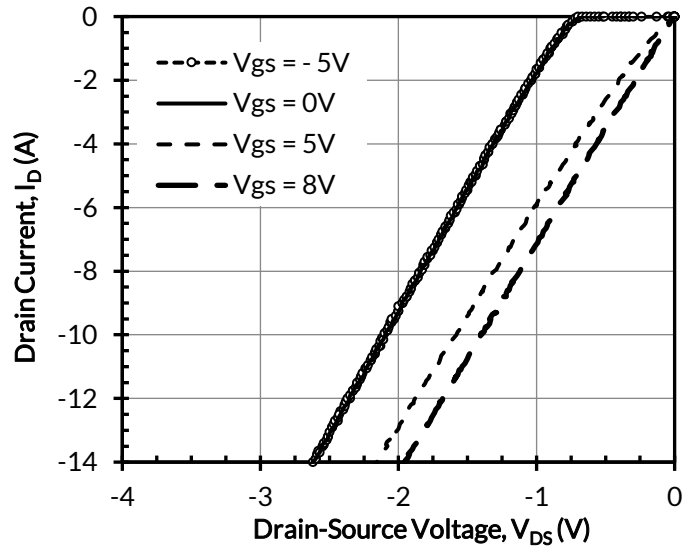


Figure 10. 3rd quadrant characteristics at $T_j = 25^\circ\text{C}$

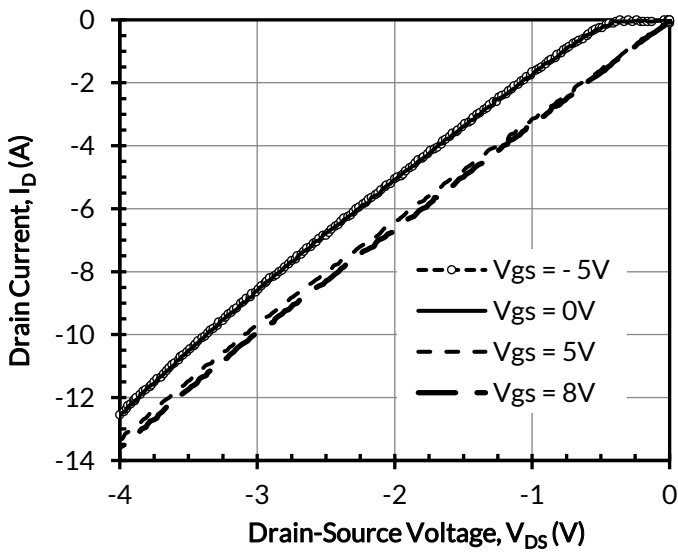


Figure 11. 3rd quadrant characteristics at $T_j = 175^\circ\text{C}$

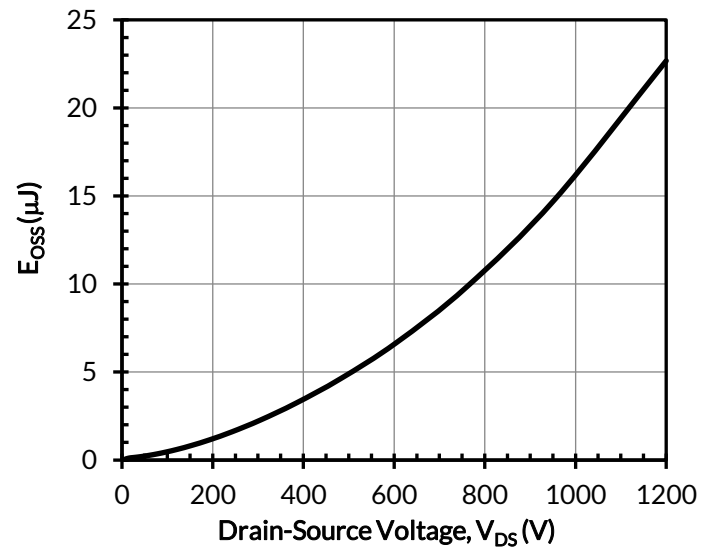


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$

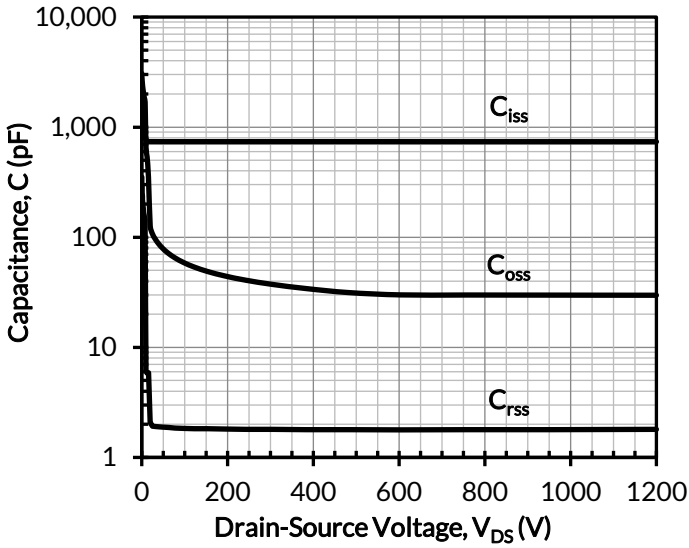


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

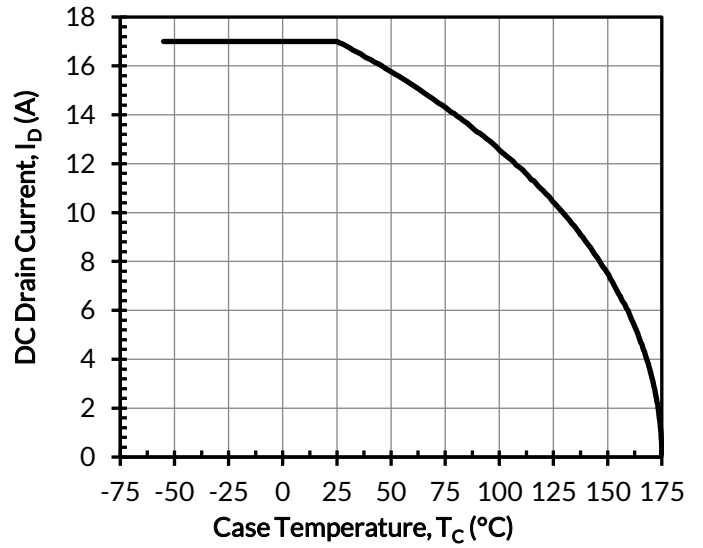


Figure 14. DC drain current derating

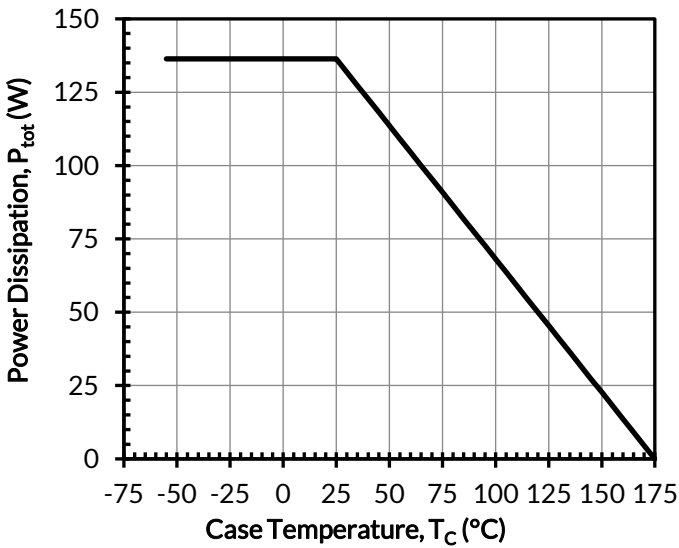


Figure 15. Total power dissipation

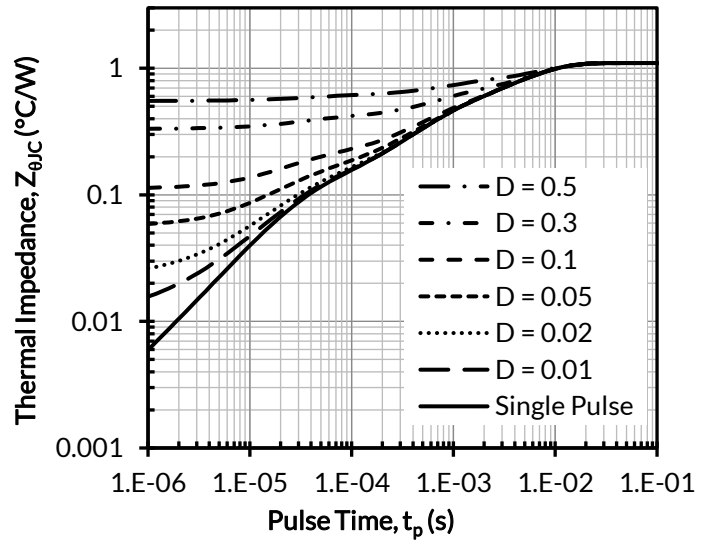


Figure 16. Maximum transient thermal impedance

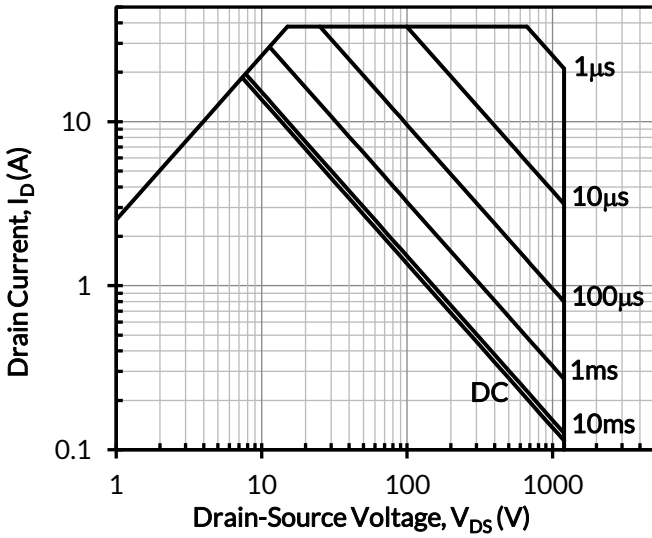


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

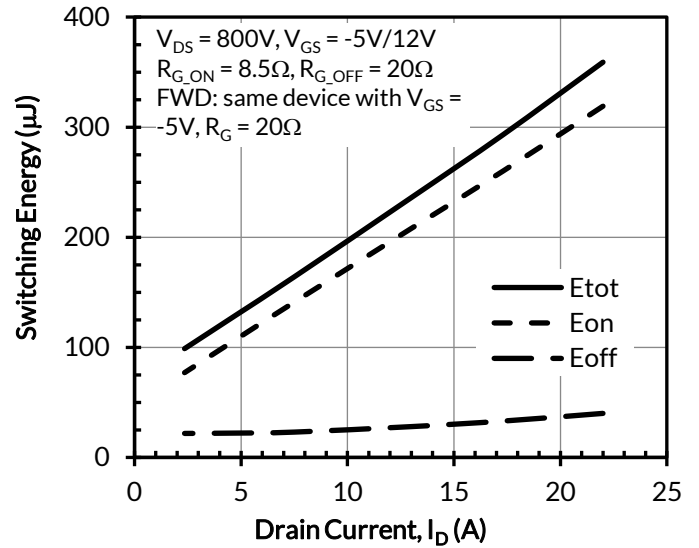


Figure 18. Clamped inductive switching energy vs. drain current at $T_J = 25^\circ\text{C}$

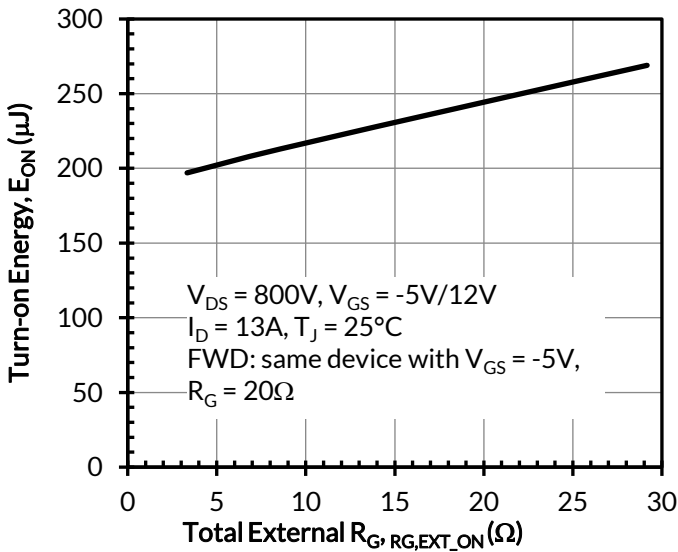


Figure 19. Clamped inductive switching turn-on energy vs. $R_{G,EXT,ON}$

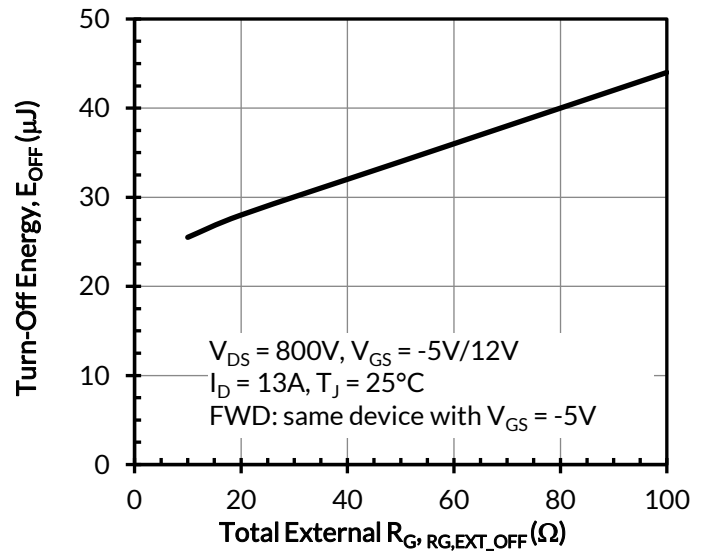


Figure 20. Clamped inductive switching turn-off energy vs. $R_{G,EXT,OFF}$

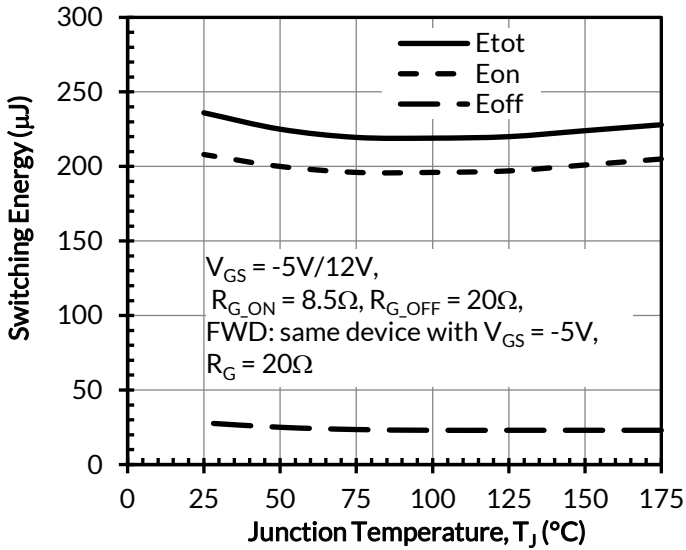


Figure 21. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 800V$ and $I_D = 13A$

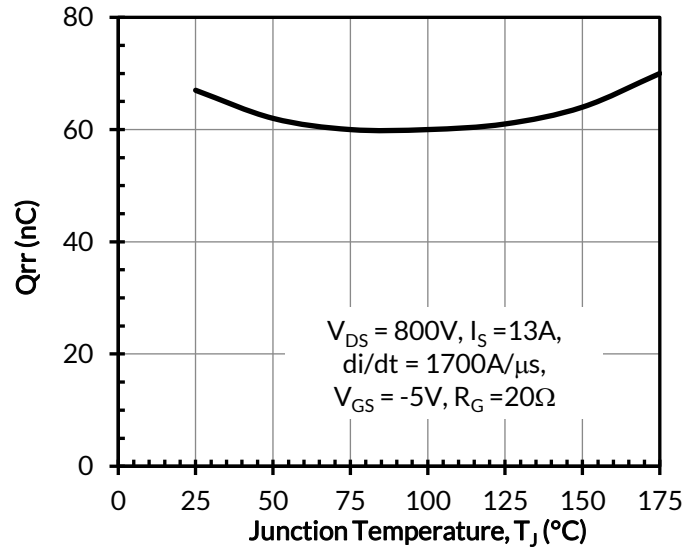


Figure 22. Reverse recovery charge Q_{rr} vs. junction temperature

Applications Information

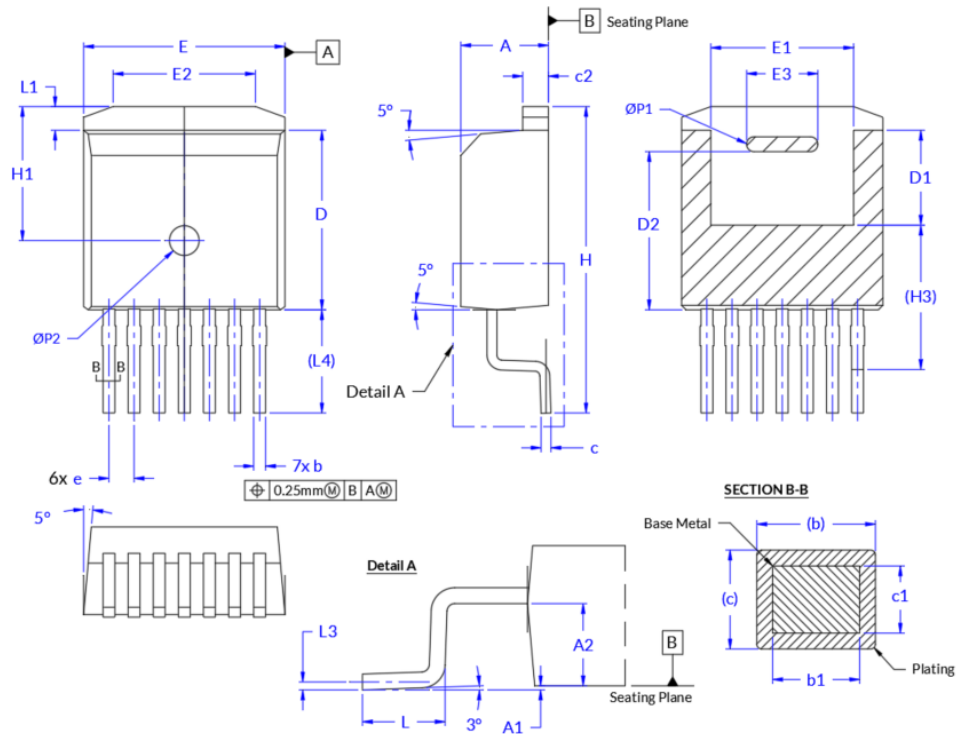
SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

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PACKAGE OUTLINE


SYM	7L-D2PAK			
	MM		MIN	MAX
A	4.30	4.56	.169	.180
A1	0.00	0.25	.000	.010
A2	2.45	2.75	.096	.108
b	0.50	0.70	.020	.028
b1	0.50	-	.020	-
c	0.40	0.60	.016	.024
c1	0.40	-	.016	-
c2	1.20	1.40	.047	.055
D	8.93	9.23	.352	.363
D1	4.65	4.95	.183	.195
D2	7.90	8.10	.311	.319
e	1.27 BSC		.050 BSC	
E	10.08	10.28	.397	.405
E1	6.82	7.62	.269	.300
E2	6.50	8.60	.256	.339
E3	3.50	3.70	.138	.146
H	15.00	16.00	.591	.630
H1	6.68	6.88	.263	.271
H3	7.3 REF.		.287 REF	
L	1.90	2.50	.075	.098
L1	0.98	1.42	.039	.056
L3	0.25 BSC		.0098 BSC	
L4	5.22 REF		.205 REF	
ØP1	0.65	0.85	.026	.033
ØP2	1.40	1.60	.055	.063

Notes:

1. GENERAL TOLERANCE: ± 0.1 unless otherwise specified
2. CONTROLLING DIMENSION: **MILLIMETERS**
3. PACKAGE BODY SIDES EXCLUDE MOLD FLASH AND GATE BURRS.
4. DIMENSION L IS MEASURED IN GAUGE LINE.
5. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
6. DIMENSION c1 AND b1 APPLIES TO BASE METAL ONLY

PART MARKING

G3, 650V / 1200V variant

UF3C: > 40 mOhm

UF3SC: ≤ 40 mOhm

G3, 1700V variant

UF3N: 400 mOhm

G4, 750V variant

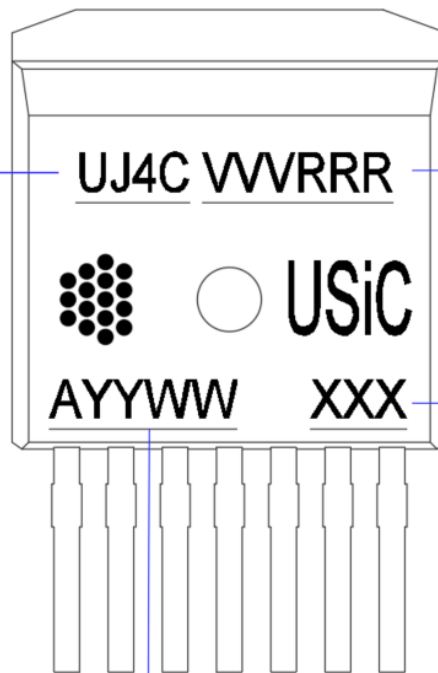
UJ4C: ≥ 23 mOhm

UJ4SC: < 23 mOhm

G4, 1200V variant

UF4C: > 30 mOhm

UF4SC: ≤ 30 mOhm



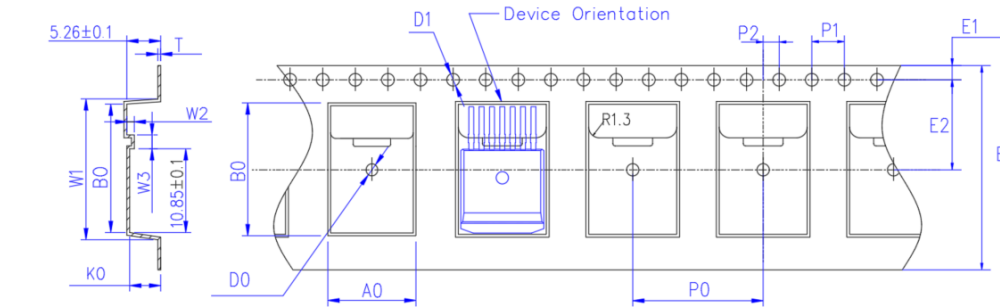
VVV : Voltage Rating
 RRR : Resistance Rating

Lot Code

A: Assembly Site
 YY: Year Code
 WW: Week code

PACKING TYPE

Carrier Tape

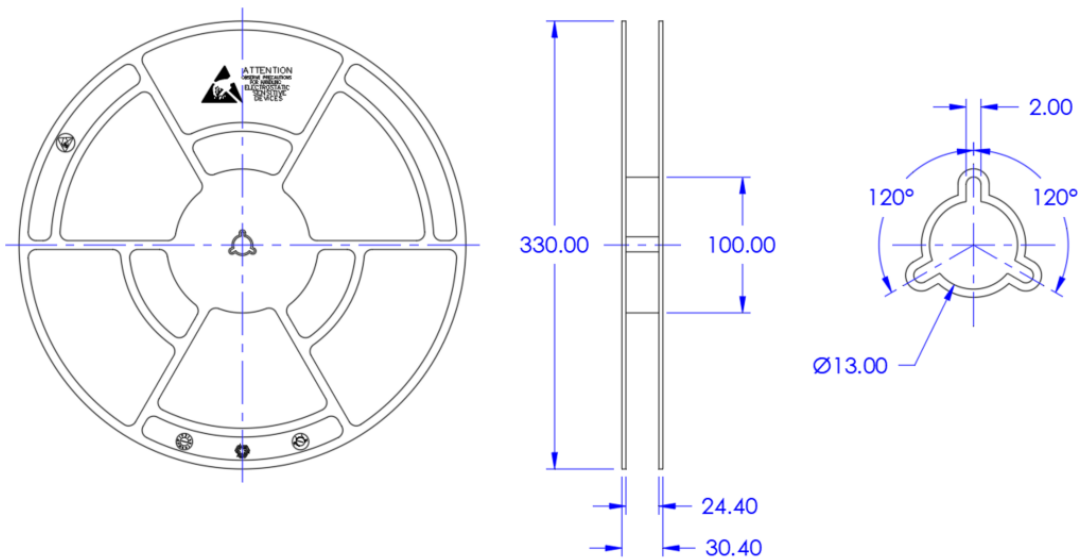


UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
D2PAK (24 mm)	10.80 ±0.10	16.30 ±0.10	4.70 ±0.10	1.50 ±0.10	1.50 $\begin{smallmatrix} +0.1 \\ -0 \end{smallmatrix}$	24.00 ±0.30	1.75 ±0.10	11.50 ±0.10	16.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.35 ±0.10

Exterior size	
Spec 1	W1 16.9±0.1
	W2 1.3±0.1
	W3 1.0±0.1
Spec 2	W1 17.2±0.1 (a)
	W2 1.8±0.1 (b)
	W3 0.85±0.1 (c)

Reel



All dimensions in millimeters
 Anti-Static Tape and Reel (T&R)
 Quantity per Reel: 800 units



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REVISION HISTORY

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
C	11/06/2023	Updated to Qorvo template Updated Package outline drawing based latest drawing revision	Glenn Galang
D	05/21/2024	Added illustration of device orientation on carrier tape (page 3)	Glenn Galang

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