

QORVO

SiC JFET Division

Is Now Part of

onsemi™

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

DATASHEET

UF3C065080B3

Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, D²PAK-3L, 650 V, 80 mohm

Rev. C, January 2025

Description

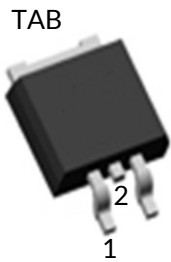
This SiC FET device is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D²PAK-3L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads when used with recommended RC-snubbers, and any application requiring standard gate drive.

Features

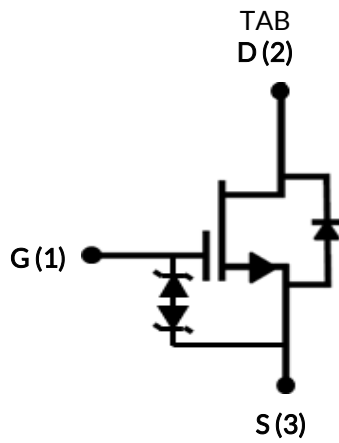
- ◆ Typical on-resistance $R_{DS(on),typ}$ of 80mΩ
- ◆ Maximum operating temperature of 175°C
- ◆ Excellent reverse recovery
- ◆ Low gate charge
- ◆ Low intrinsic capacitance
- ◆ ESD protected, HBM class 2
- ◆ Very low switching losses (required RC-snubber loss negligible under typical operating conditions)

Typical applications

- ◆ EV charging
- ◆ PV inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating



3



Part Number	Package	Marking
UF3C065080B3	D ² PAK-3L	UF3C065080B3



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current ¹	I_D	$T_C = 25^\circ\text{C}$	25	A
		$T_C = 100^\circ\text{C}$	18.2	A
Pulsed drain current ²	I_{DM}	$T_C = 25^\circ\text{C}$	65	A
Single pulsed avalanche energy ³	E_{AS}	$L=15\text{mH}, I_{AS}=2.1\text{A}$	33	mJ
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	115	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Reflow soldering temperature	T_{solder}	reflow MSL 1	245	$^\circ\text{C}$

1. Limited by $T_{J,max}$

2. Pulse width t_p limited by $T_{J,max}$

3. Starting $T_J = 25^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			1	1.3	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0V, I_D=1mA$	650			V
Total drain leakage current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V, T_J=25^\circ\text{C}$		6	100	μA
		$V_{DS}=650V, V_{GS}=0V, T_J=175^\circ\text{C}$		40		
Total gate leakage current	I_{GSS}	$V_{DS}=0V, T_J=25^\circ\text{C}, V_{GS}=-20V / +20V$		6	± 20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=20A, T_J=25^\circ\text{C}$		80	100	m Ω
		$V_{GS}=12V, I_D=20A, T_J=175^\circ\text{C}$		141		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	4	5	6	V
Gate resistance	R_G	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C=25^\circ\text{C}$			25	A
Diode pulse current ²	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			65	A
Forward voltage	V_{FSD}	$V_{GS}=0V, I_S=10A, T_J=25^\circ\text{C}$		1.5	2	V
		$V_{GS}=0V, I_S=10A, T_J=175^\circ\text{C}$		1.75		
Reverse recovery charge	Q_{rr}	$V_R=400V, I_S=20A, V_{GS}=-5V, R_{G,EXT}=10\Omega, di/dt=2200A/\mu\text{s}, T_J=25^\circ\text{C}$		119		nC
Reverse recovery time	t_{rr}	$T_J=25^\circ\text{C}$		16		ns
Reverse recovery charge	Q_{rr}	$V_R=400V, I_S=20A, V_{GS}=-5V, R_{G,EXT}=10\Omega, di/dt=2200A/\mu\text{s}, T_J=150^\circ\text{C}$		73		nC
Reverse recovery time	t_{rr}	$T_J=150^\circ\text{C}$		11		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units	
			Min	Typ	Max		
Input capacitance	C_{iss}	$V_{DS}=100V, V_{GS}=0V$ $f=100kHz$		1500		pF	
Output capacitance	C_{oss}			104			
Reverse transfer capacitance	C_{rss}			2.6			
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		77		pF	
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		176		pF	
C_{oss} stored energy	E_{oss}	$V_{DS}=400V, V_{GS}=0V$		6.2		μJ	
Total gate charge	Q_G	$V_{DS}=400V, I_D=20A,$ $V_{GS} = -5V$ to 15V		51		nC	
Gate-drain charge	Q_{GD}			11			
Gate-source charge	Q_{GS}			19			
Turn-on delay time	$t_{d(on)}$	$V_{DS}=400V, I_D=20A,$ Gate Driver = -5V to +15V, Turn-on $R_{G,EXT}=1\Omega,$ Turn-off $R_{G,EXT}=22\Omega$ Inductive Load, FWD: same device with $V_{GS} = -5V$ and $R_G = 22\Omega,$ RC snubber: $R_S=5\Omega$ and $C_S=100pF, T_J=25^\circ C$		25		ns	
Rise time	t_r			13			
Turn-off delay time	$t_{d(off)}$			50			
Fall time	t_f			12			
Turn-on energy including R_S energy ⁴	E_{ON}			164			μJ
Turn-off energy including R_S energy ⁴	E_{OFF}			24			
Total switching energy including R_S energy ⁴	E_{TOTAL}			188			
Snubber R_S energy during turn-on	$E_{RS,ON}$			0.95			
Snubber R_S energy during turn-off	$E_{RS,OFF}$			1.52			
Turn-on delay time	$t_{d(on)}$			20			
Rise time	t_r		13				
Turn-off delay time	$t_{d(off)}$		52				
Fall time	t_f		12				
Turn-on energy including R_S energy ⁴	E_{ON}		140		μJ		
Turn-off energy including R_S energy ⁴	E_{OFF}		23				
Total switching energy including R_S energy ⁴	E_{TOTAL}		163				
Snubber R_S energy during turn-on	$E_{RS,ON}$		0.93				
Snubber R_S energy during turn-off	$E_{RS,OFF}$		1.43				

4. The switching performance are evaluated with a RC snubber circuit as shown in Figure 24.

Typical Performance Diagrams

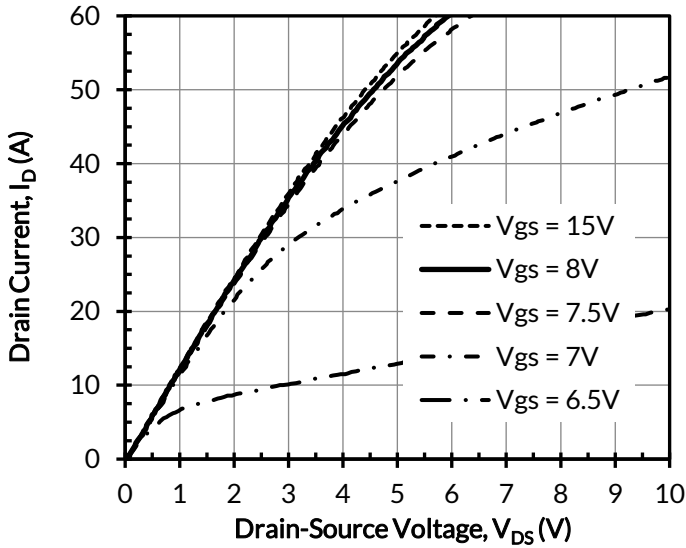


Figure 1. Typical output characteristics at $T_J = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

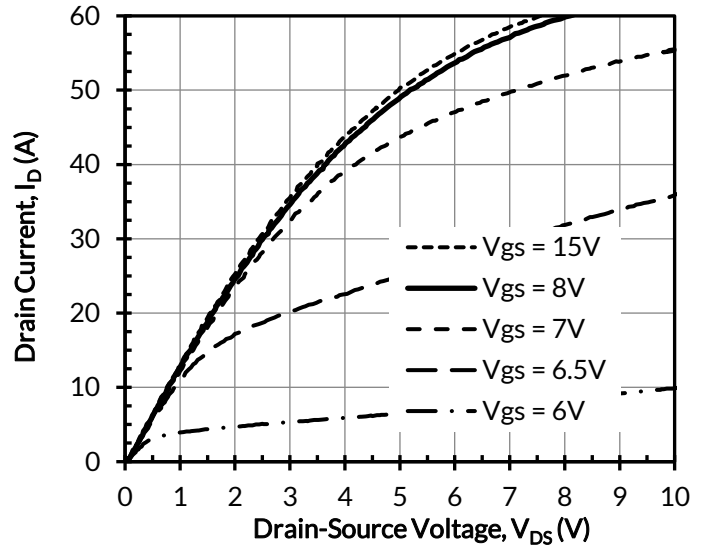


Figure 2. Typical output characteristics at $T_J = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

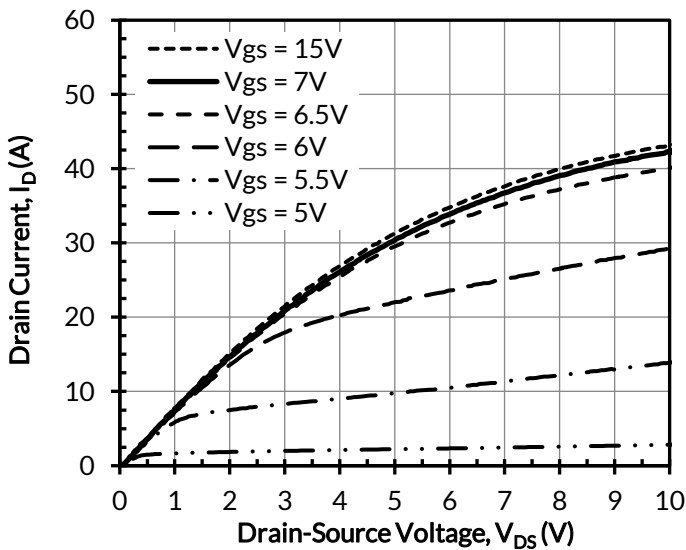


Figure 3. Typical output characteristics at $T_J = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

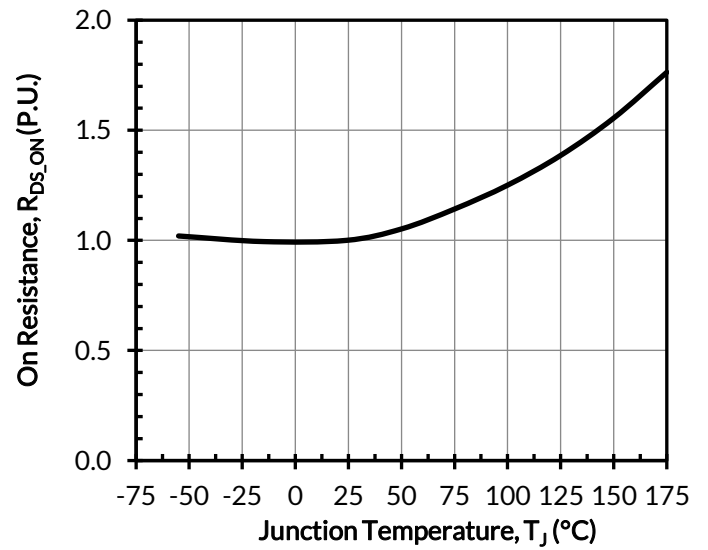


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 20\text{A}$

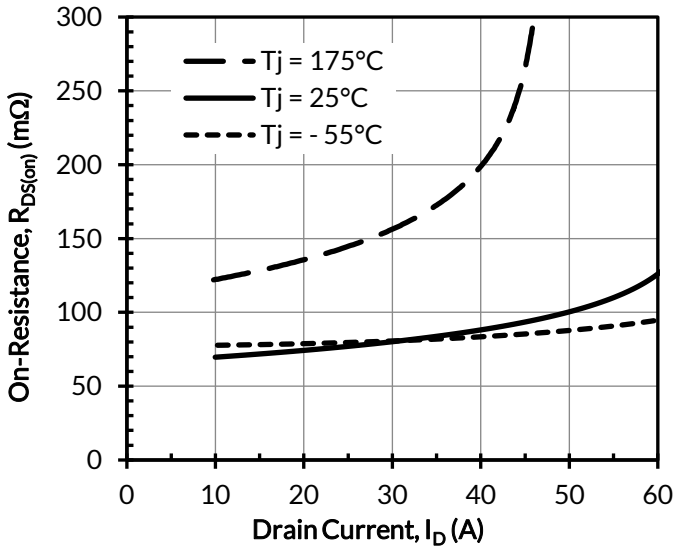


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12\text{V}$

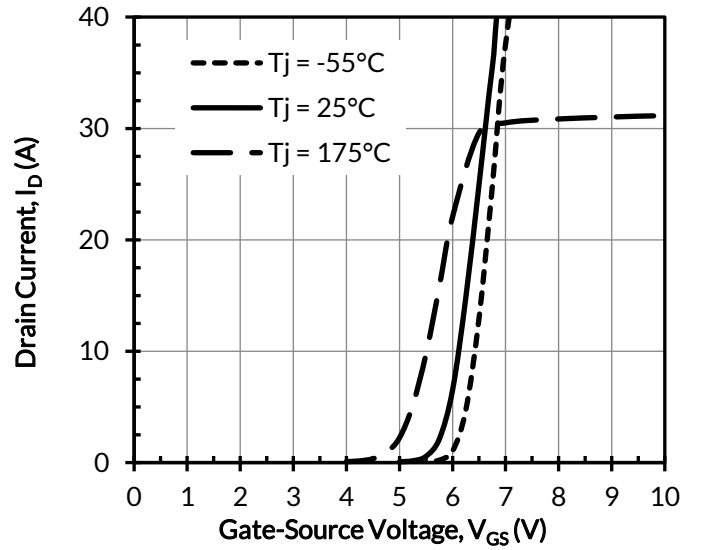


Figure 6. Typical transfer characteristics at $V_{DS} = 5\text{V}$

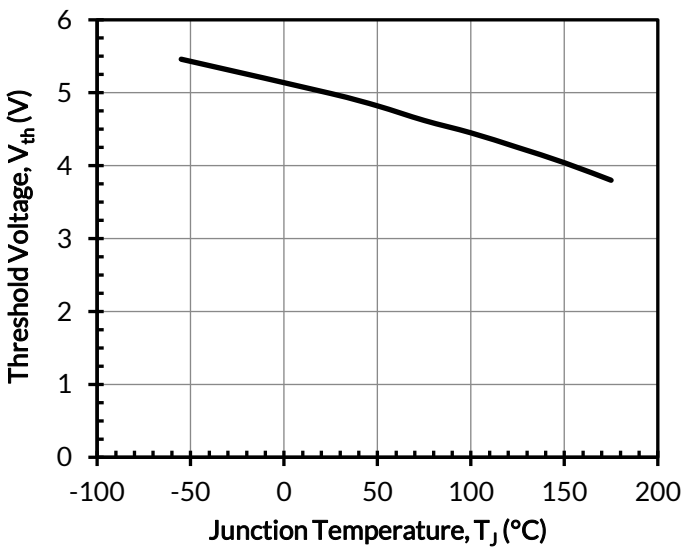


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5\text{V}$ and $I_D = 10\text{mA}$

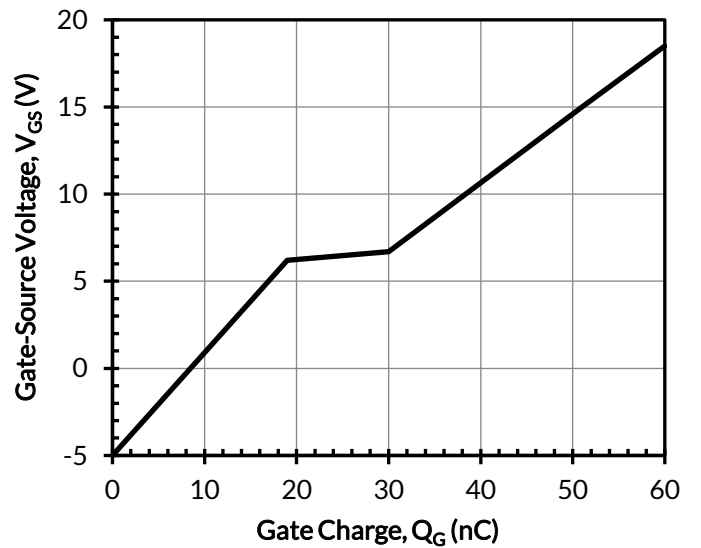


Figure 8. Typical gate charge at $V_{DS} = 400\text{V}$ and $I_D = 20\text{A}$

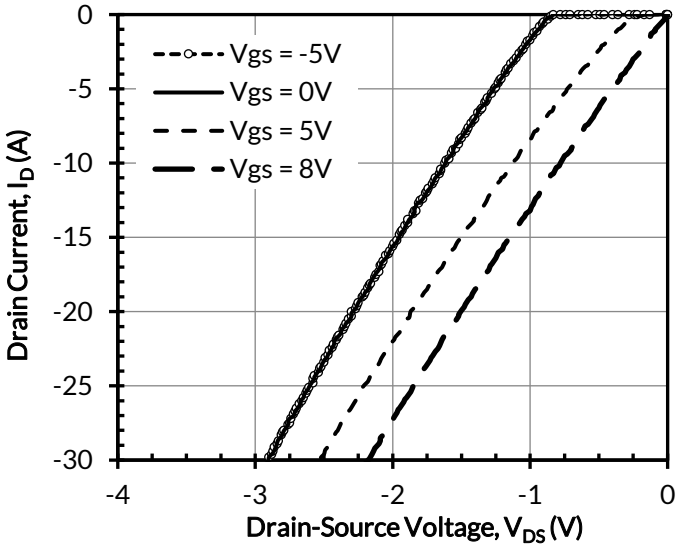


Figure 9. 3rd quadrant characteristics at $T_j = -55^\circ\text{C}$

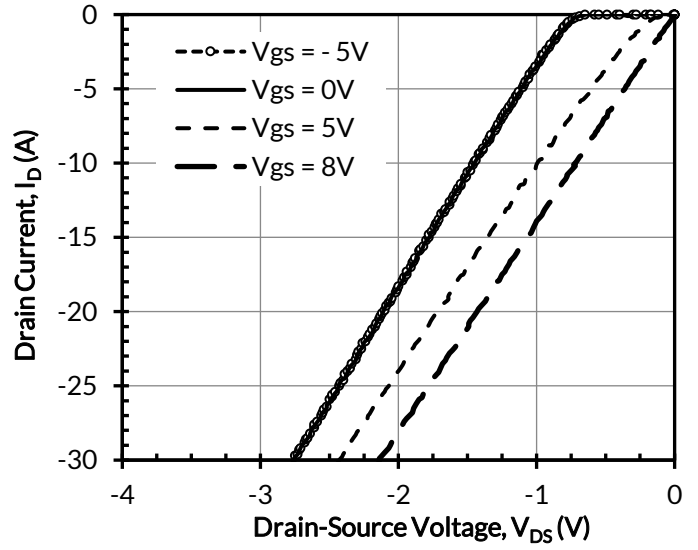


Figure 10. 3rd quadrant characteristics at $T_j = 25^\circ\text{C}$

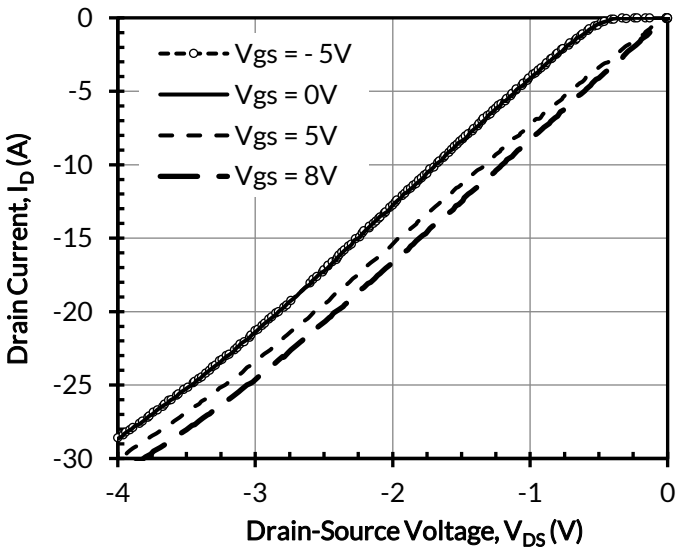


Figure 11. 3rd quadrant characteristics at $T_j = 175^\circ\text{C}$

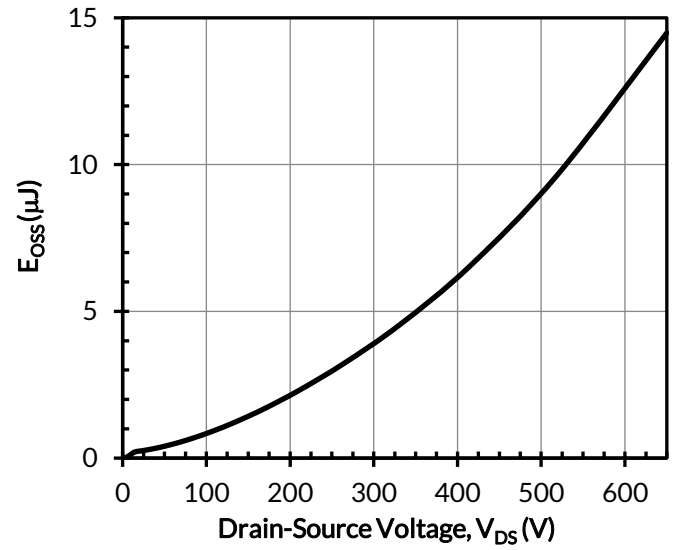


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$

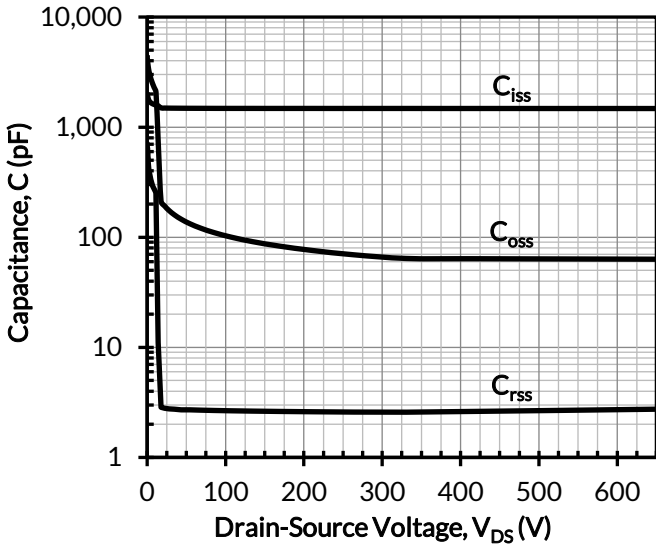


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

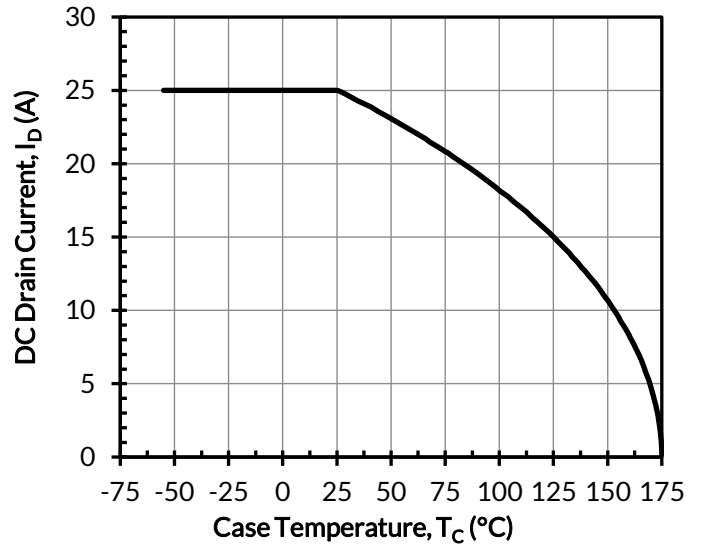


Figure 14. DC drain current derating

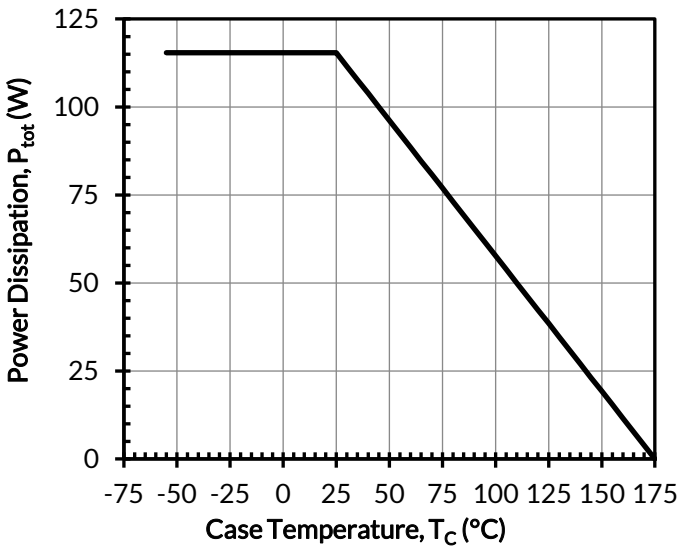


Figure 15. Total power dissipation

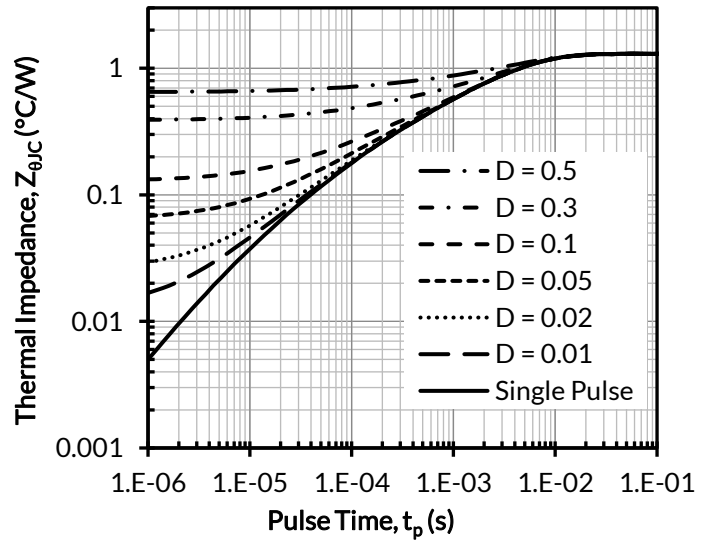


Figure 16. Maximum transient thermal impedance

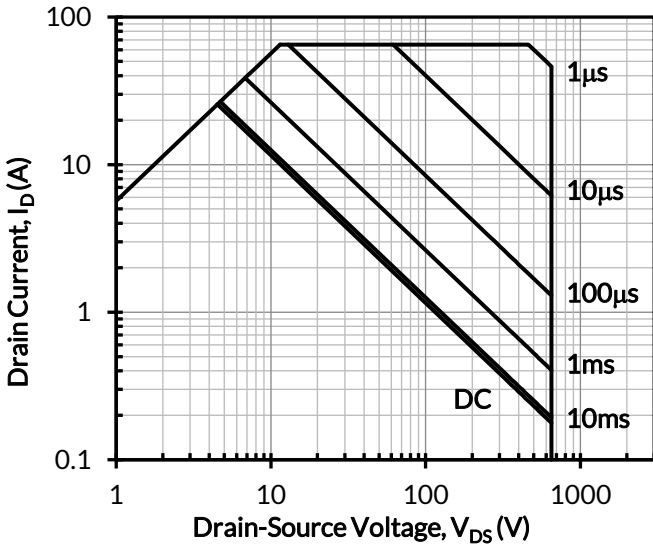


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

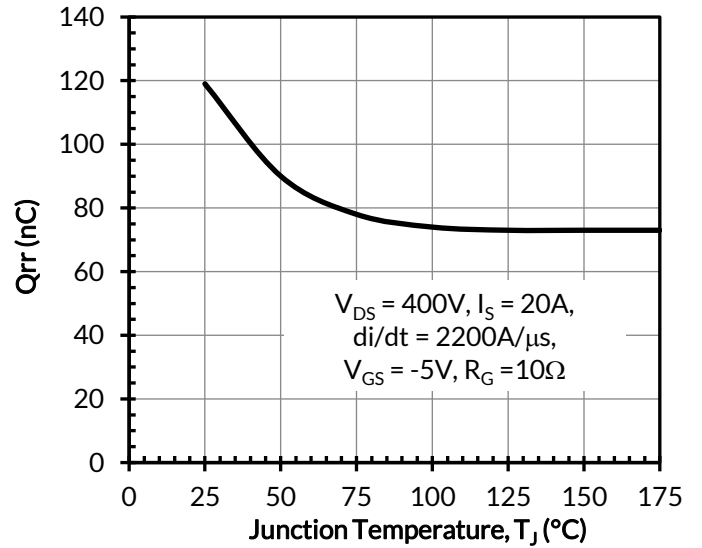
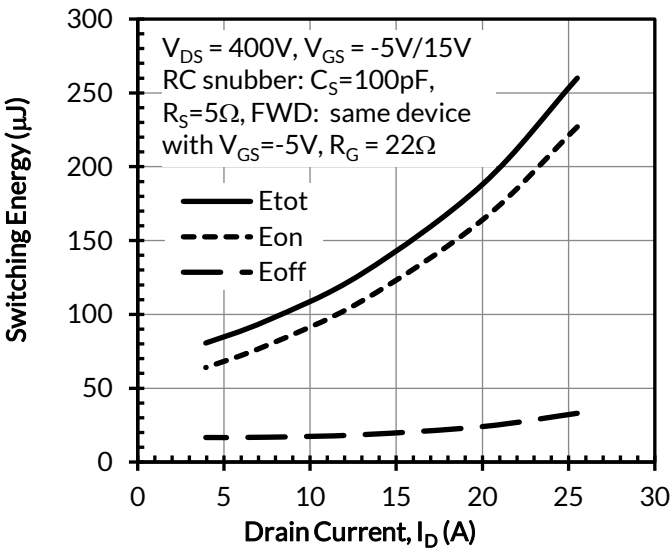
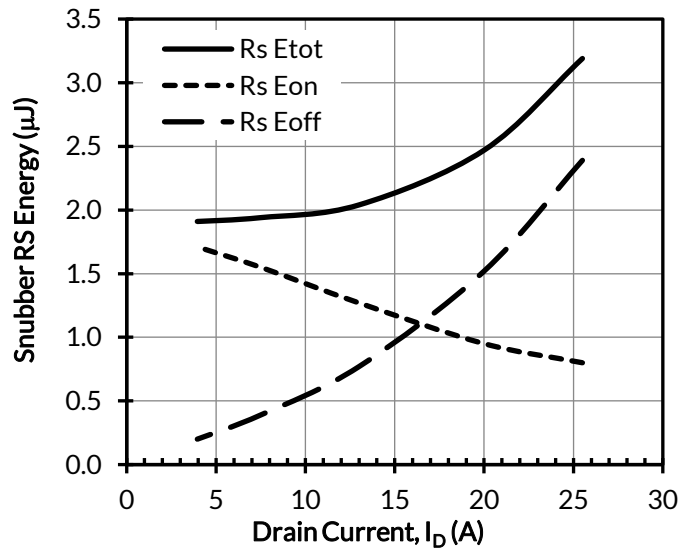


Figure 18. Reverse recovery charge Q_{rr} vs. junction temperature

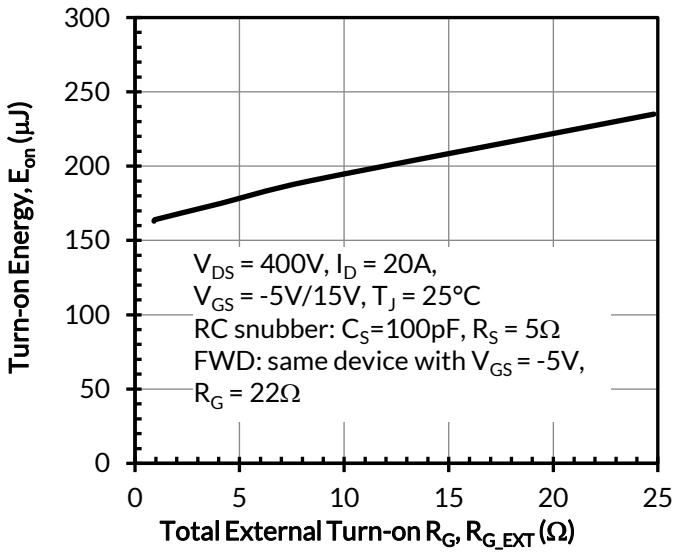


(a)

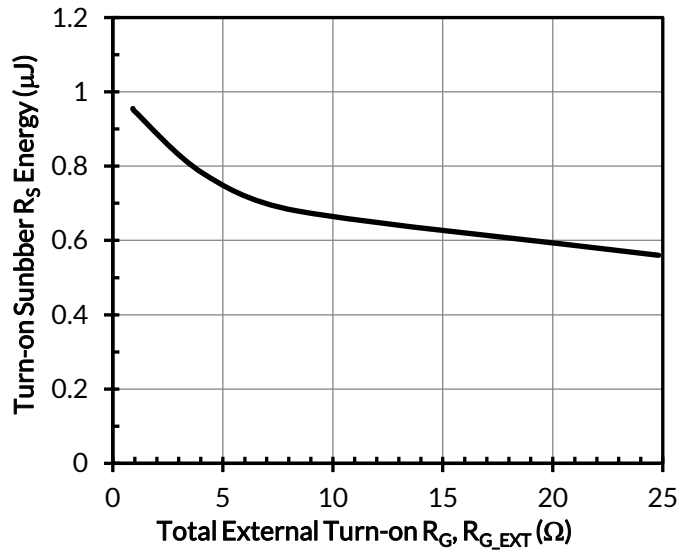


(b)

Figure 19. Clamped inductive switching energy (a) and RC snubber energy loss (b) vs. drain current at $T_J = 25^\circ\text{C}$, turn-on $R_{G,EXT} = 1\Omega$, and turn-off $R_{G,EXT} = 22\Omega$

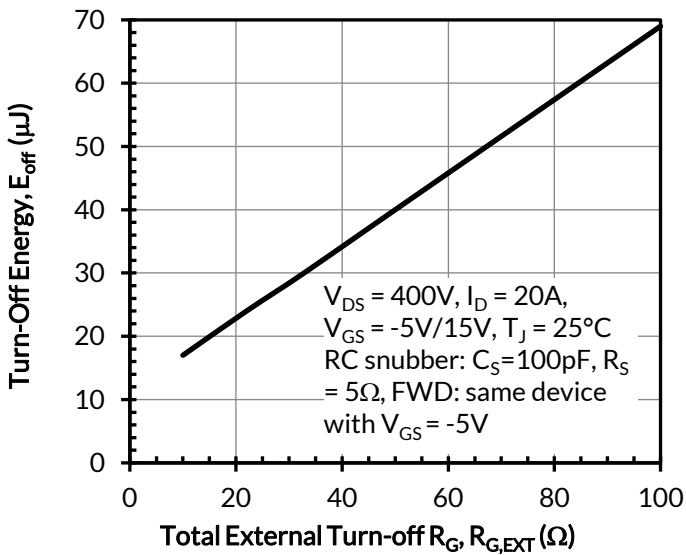


(a)

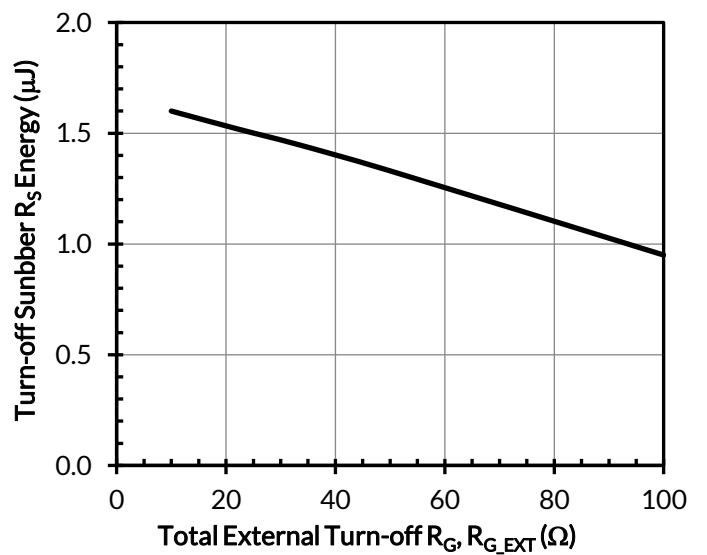


(b)

Figure 20. Clamped inductive switching turn-on energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of total external turn-on gate resistor R_{G_EXT}

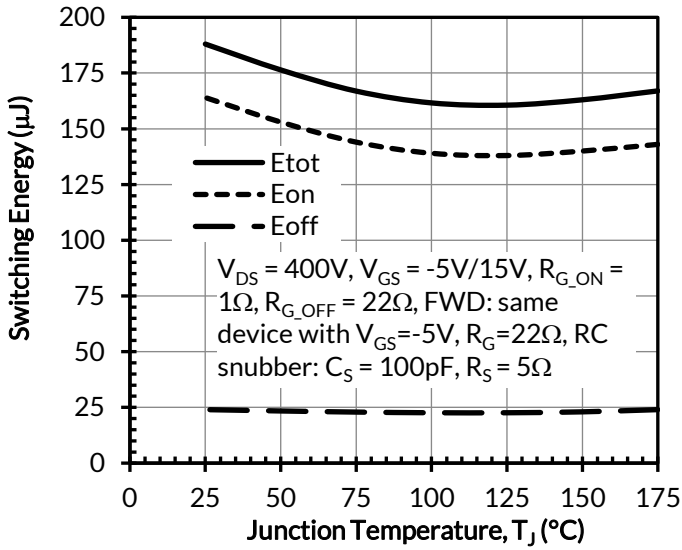


(a)

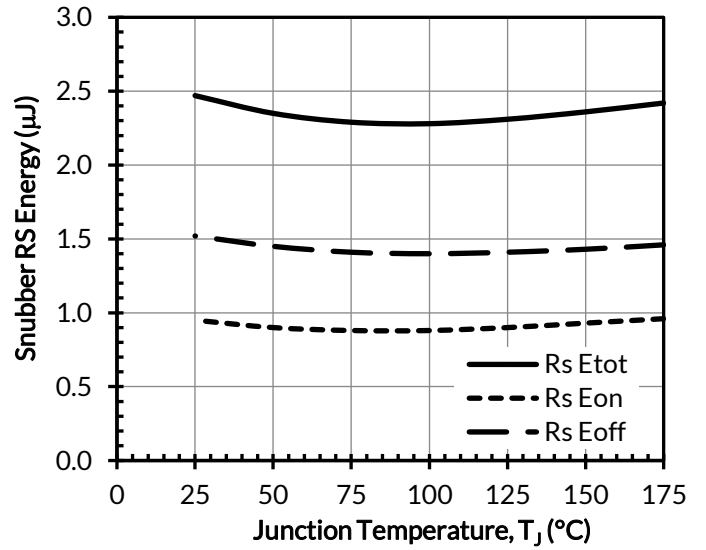


(b)

Figure 21. Clamped inductive switching turn-off energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of total external turn-off gate resistor R_{G_EXT}

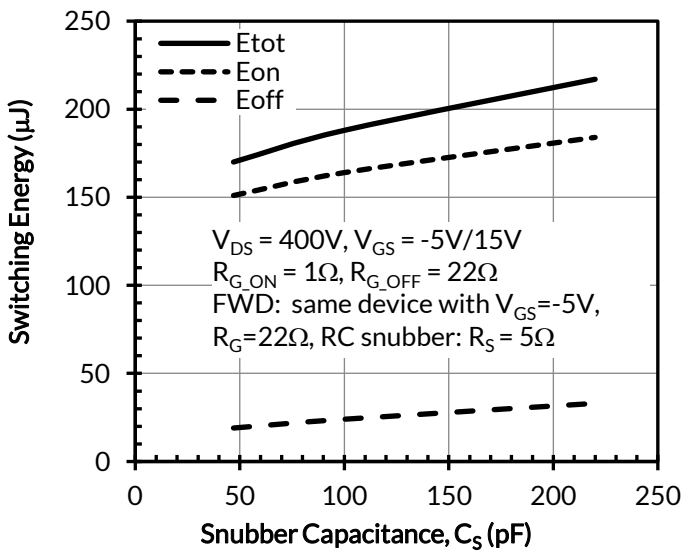


(a)

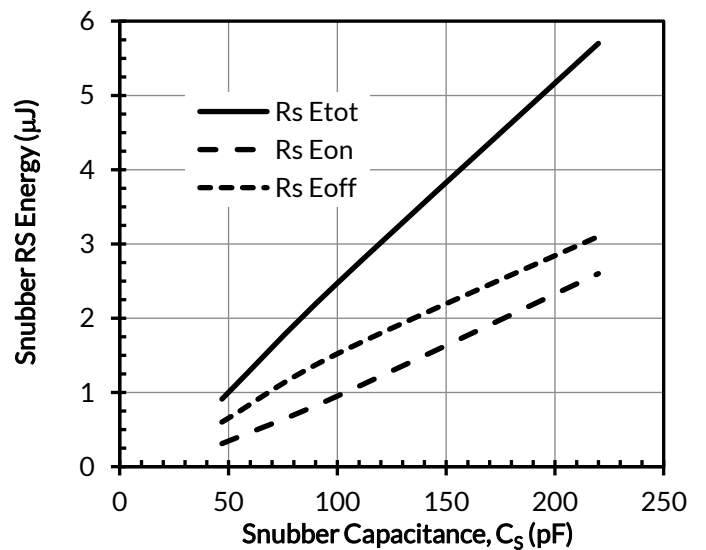


(b)

Figure 22. Clamped inductive switching energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of junction temperature at $I_D = 20A$



(a)



(b)

Figure 23. Clamped inductive switching energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of snubber capacitance at $I_D = 20A$ and $T_J = 25^\circ C$

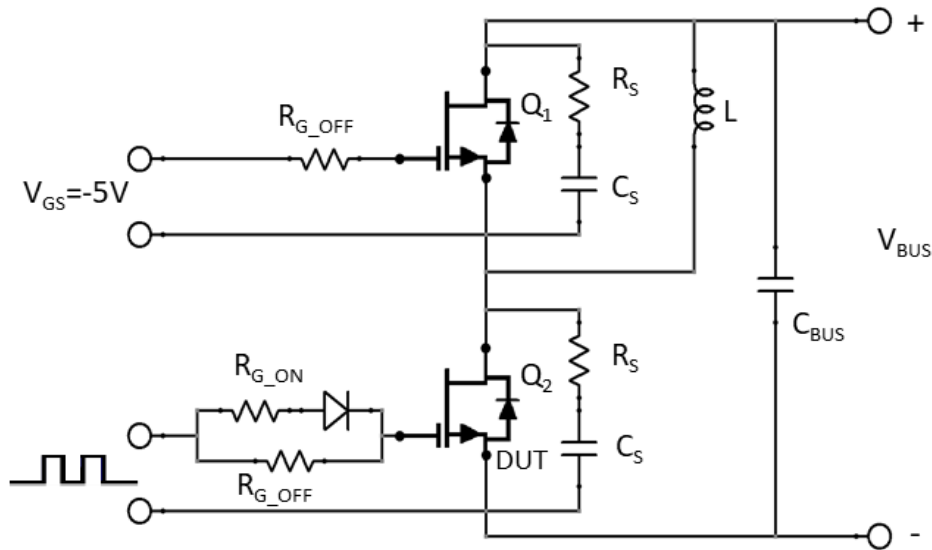


Figure 24. Clamped inductive load switching test circuit
 An RC snubber ($R_S = 5\Omega$ and $C_S = 100\text{pF}$) is required to improve the turn-off waveforms.

Applications Information

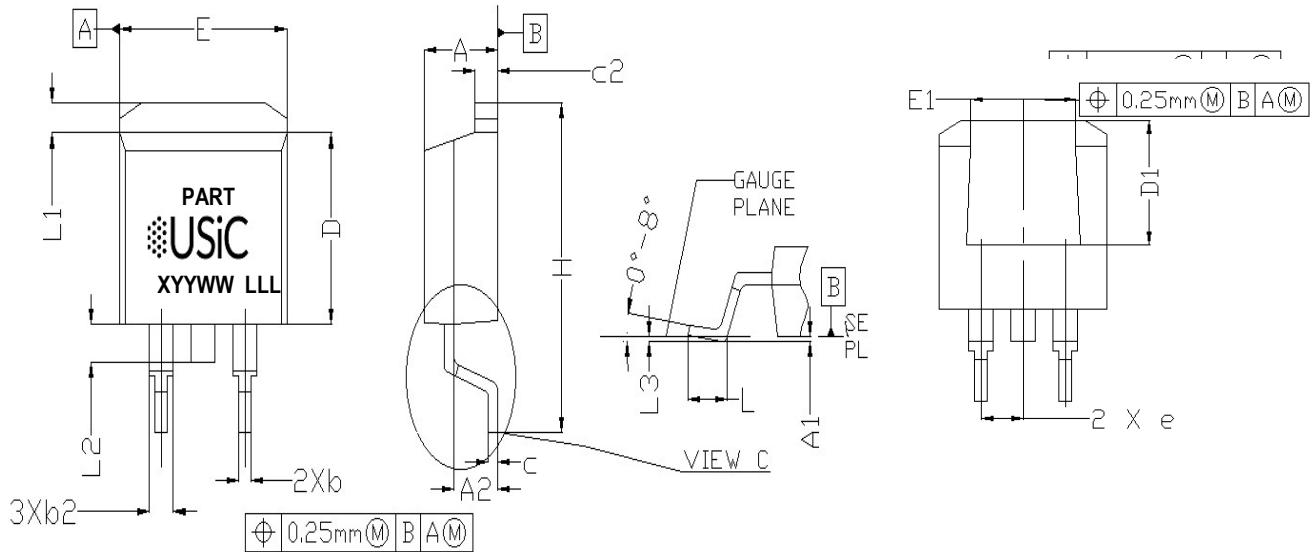
SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

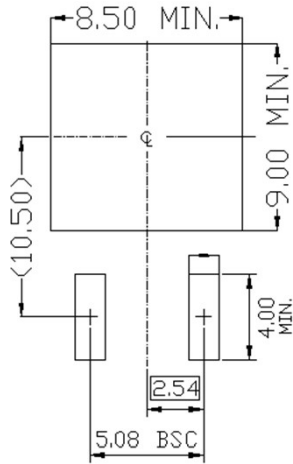
A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

Important notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.

PACKAGE OUTLINE


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.190	4.064	4.826
A1	0.000	0.010	0.00	0.254
A2	0.087	0.114	2.20	2.8956
b	0.020	0.039	0.508	0.9906
b2	0.045	0.07	1.143	1.778
c	0.015	0.029	0.381	0.7366
c2	0.045	0.065	1.143	1.651
D	0.330	0.380	8.382	9.652
D1	0.270	0.330	6.858	8.37
e	0.100 BSC		2.54 BSC	
E	0.380	0.420	9.652	10.668
E1	0.245	0.330	6.223	8.37
H	0.575	0.625	14.605	15.875
L	0.070	0.110	1.778	2.794
L1	0.040	0.066	1.02	1.6764
L2	0.050	0.07	1.27	1.778
L3	0.010 BSC		0.25 BSC	

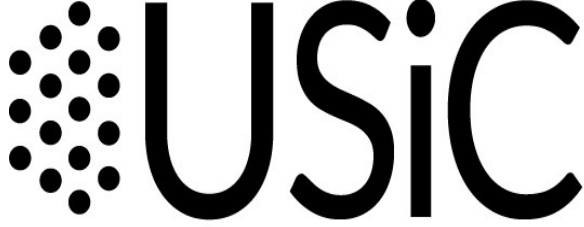
PCB LAND PATTERN

Notes:

1. PACKAGE BODY SIDES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.10MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. DIMENSION L IS MEASURED IN GAUGE LINE.
4. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-263AB.

PART MARKING

PART NUMBER



XY Y WW L L L

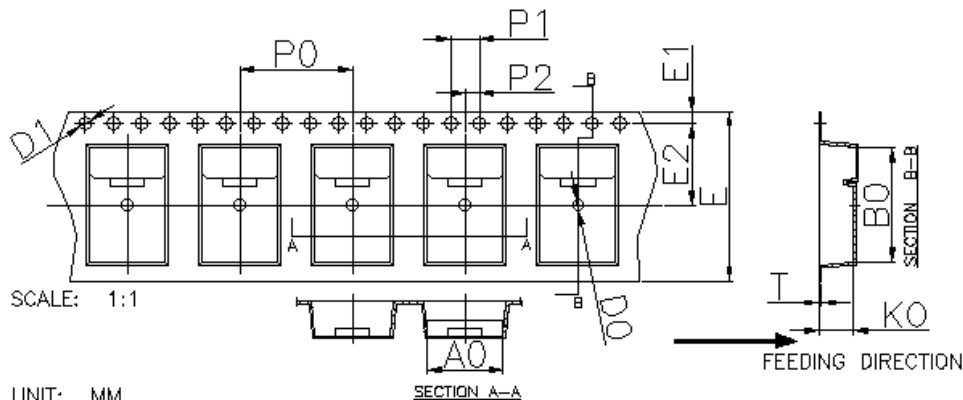
PART NUMBER = REFER TO
DS_PN DECODER FOR DETAILS

X = ASSEMBLY SITE
YY = YEAR
WW = WORK WEEK
LLL = LOT ID

PACKING TYPE

ANTI-STATIC TAPE & REEL (T&R)

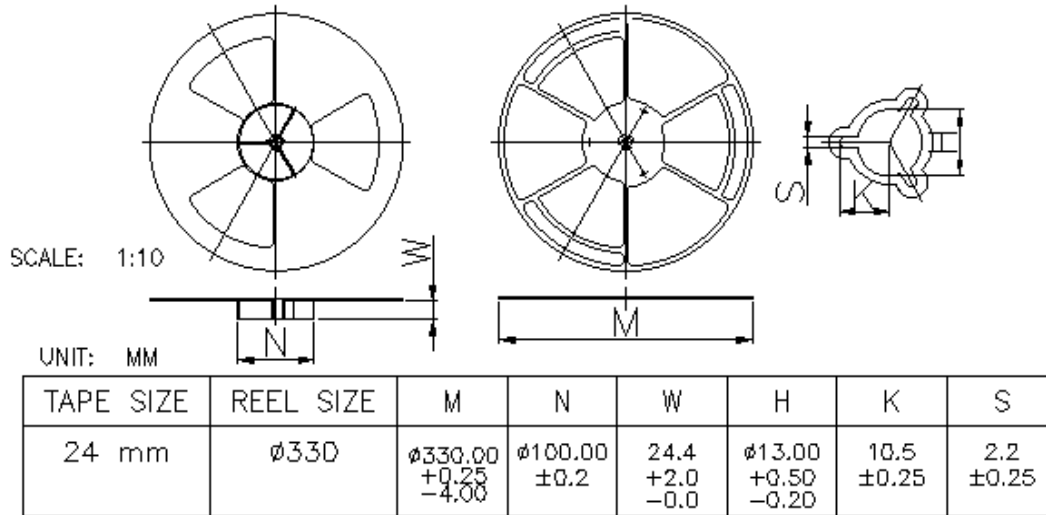
QUANTITY /REEL : 800 UNITS

CARRIER TAPE DRAWING


PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
D2PAK (24 mm)	10.80 ±0.10	16.30 ±0.10	4.70 ±0.10	1.50 ±0.10	1.50 ±0.1	24.00 ±0.30	1.75 ±0.10	11.50 ±0.10	16.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.35 ±0.10

NOTE:

- 1.Measured from centeline of sprocket hole to centrelines of pocket.
- 2.Cumulative tolerance of 10 sprocket holes is ±0.20.
- 3.Camber not to exceed 2mm in 200mm

REEL DRAWING

DISCLAIMER

United Silicon Carbide, Inc. reserves the right to change or modify any of the products and their inherent physical and technical specifications without prior notice. United Silicon Carbide, Inc. assumes no responsibility or liability for any errors or inaccuracies within.

Information on all products and contained herein is intended for description only. No license, express or implied, to any intellectual property rights is granted within this document.

United Silicon Carbide, Inc. assumes no liability whatsoever relating to the choice, selection or use of the United Silicon Carbide, Inc. products and services described herein.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales