

QORVO

SiC JFET Division

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Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, TO-247-4L, 650 V, 27 mohm

DATASHEET

UF3C065030K4S

Rev. B, January 2025

Description

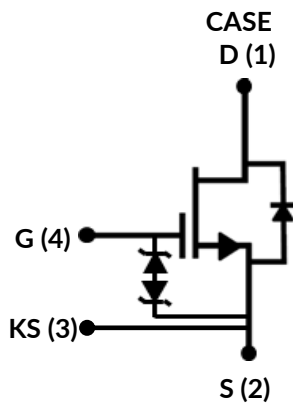
United Silicon Carbide's cascode products co-package its high-performance F3 SiC fast JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits very fast switching using a 4-terminal TO-247-package and the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads, and any application requiring standard gate drive.

Features

- ◆ Typical on-resistance $R_{DS(on),typ}$ of 27m Ω
- ◆ Maximum operating temperature of 175°C
- ◆ Excellent reverse recovery
- ◆ Low gate charge
- ◆ Low intrinsic capacitance
- ◆ ESD protected, HBM class 2
- ◆ TO-247-4L package for faster switching, clean gate waveforms

Typical applications

- ◆ EV charging
- ◆ PV inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating



Part Number	Package	Marking
UF3C065030K4S	TO-247-4L	UF3C065030K4S



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current ¹	I_D	$T_C = 25^\circ\text{C}$	85	A
		$T_C = 100^\circ\text{C}$	62	A
Pulsed drain current ²	I_{DM}	$T_C = 25^\circ\text{C}$	230	A
Single pulsed avalanche energy ³	E_{AS}	$L=15\text{mH}, I_{AS}=4\text{A}$	120	mJ
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	441	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	$^\circ\text{C}$

1. Limited by $T_{J,max}$

2. Pulse width t_p limited by $T_{J,max}$

3. Starting $T_J = 25^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.26	0.34	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0V, I_D=1mA$	650			V
Total drain leakage current	I_{DSS}	$V_{DS}=650V,$ $V_{GS}=0V, T_J=25^\circ\text{C}$		6	150	μA
		$V_{DS}=650V,$ $V_{GS}=0V, T_J=175^\circ\text{C}$		30		
Total gate leakage current	I_{GSS}	$V_{DS}=0V, T_J=25^\circ\text{C},$ $V_{GS}=-20V / +20V$		6	± 20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=50A,$ $T_J=25^\circ\text{C}$		27	35	$\text{m}\Omega$
		$V_{GS}=12V, I_D=50A,$ $T_J=175^\circ\text{C}$		43		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	4	5	6	V
Gate resistance	R_G	$f=1\text{MHz}, \text{open drain}$		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C=25^\circ\text{C}$			85	A
Diode pulse current ²	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			230	A
Forward voltage	V_{FSD}	$V_{GS}=0V, I_F=20A,$ $T_J=25^\circ\text{C}$		1.3	1.4	V
		$V_{GS}=0V, I_F=20A,$ $T_J=175^\circ\text{C}$		1.35		
Reverse recovery charge	Q_{rr}	$V_R=400V, I_F=50A,$ $V_{GS}=-5V, R_{G,EXT}=10\Omega$ $di/dt=2650A/\mu\text{s},$ $T_J=25^\circ\text{C}$		425		nC
Reverse recovery time	t_{rr}	$V_R=400V, I_F=50A,$ $V_{GS}=-5V, R_{G,EXT}=10\Omega$ $di/dt=2650A/\mu\text{s},$ $T_J=25^\circ\text{C}$		25		ns
Reverse recovery charge	Q_{rr}	$V_R=400V, I_F=50A,$ $V_{GS}=-5V, R_{G,EXT}=10\Omega$ $di/dt=2650A/\mu\text{s},$ $T_J=150^\circ\text{C}$		280		nC
Reverse recovery time	t_{rr}	$V_R=400V, I_F=50A,$ $V_{GS}=-5V, R_{G,EXT}=10\Omega$ $di/dt=2650A/\mu\text{s},$ $T_J=150^\circ\text{C}$		20		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=100V, V_{GS}=0V$ $f=100kHz$		1500		pF
Output capacitance	C_{oss}			320		
Reverse transfer capacitance	C_{rss}			2.3		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		230		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		520		pF
C_{oss} stored energy	E_{oss}	$V_{DS}=400V, V_{GS}=0V$		18.5		μJ
Total gate charge	Q_G	$V_{DS}=400V, I_D=50A,$ $V_{GS} = -5V$ to 12V		43		nC
Gate-drain charge	Q_{GD}			11		
Gate-source charge	Q_{GS}			19		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=400V, I_D=50A,$ Gate Driver = -5V to +12V, Turn-on $R_{G,EXT}=8.5\Omega,$ Turn-off $R_{G,EXT}=20\Omega$ Inductive Load,		25		ns
Rise time	t_r			31		
Turn-off delay time	$t_{d(off)}$			48		
Fall time	t_f			12		
Turn-on energy	E_{ON}	FWD: same device with $V_{GS} = -5V, R_G = 10\Omega,$ $T_J=25^\circ C$		310		μJ
Turn-off energy	E_{OFF}			171		
Total switching energy	E_{TOTAL}			481		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=400V, I_D=50A,$ Gate Driver = -5V to +12V, Turn-on $R_{G,EXT}=8.5\Omega,$ Turn-off $R_{G,EXT}=20\Omega$ Inductive Load,		22		ns
Rise time	t_r			27		
Turn-off delay time	$t_{d(off)}$			48		
Fall time	t_f			10		
Turn-on energy	E_{ON}	FWD: same device with $V_{GS} = -5V, R_G = 10\Omega,$ $T_J=150^\circ C$		247		μJ
Turn-off energy	E_{OFF}			114		
Total switching energy	E_{TOTAL}			361		

Typical Performance Diagrams

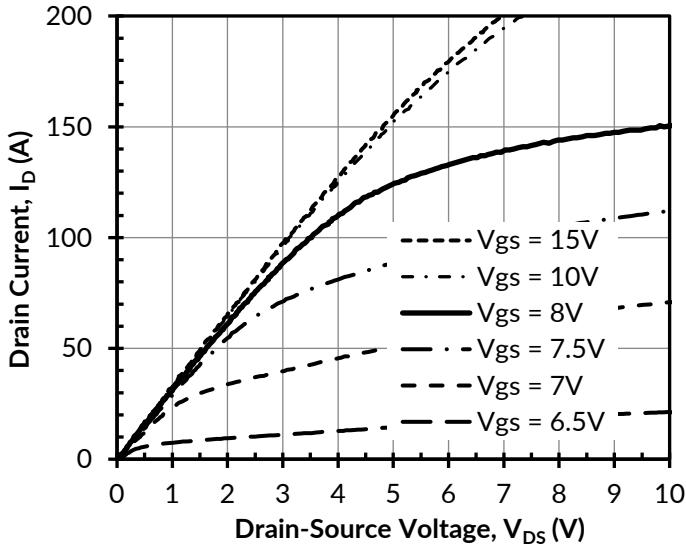


Figure 1. Typical output characteristics at $T_J = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

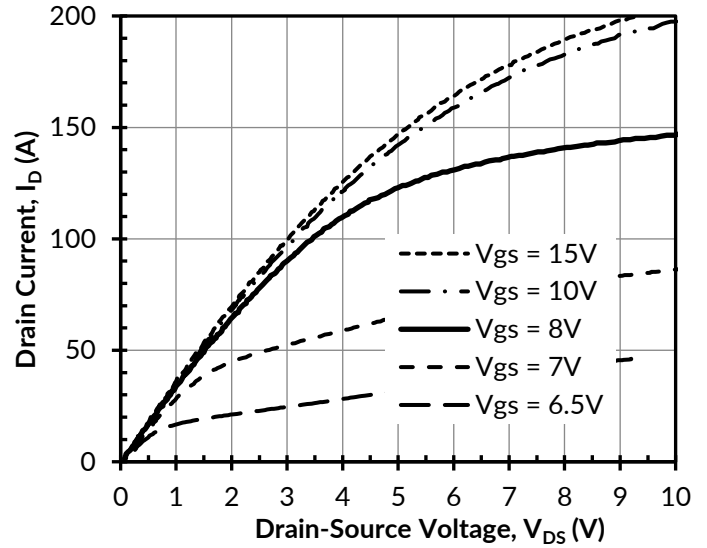


Figure 2. Typical output characteristics at $T_J = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

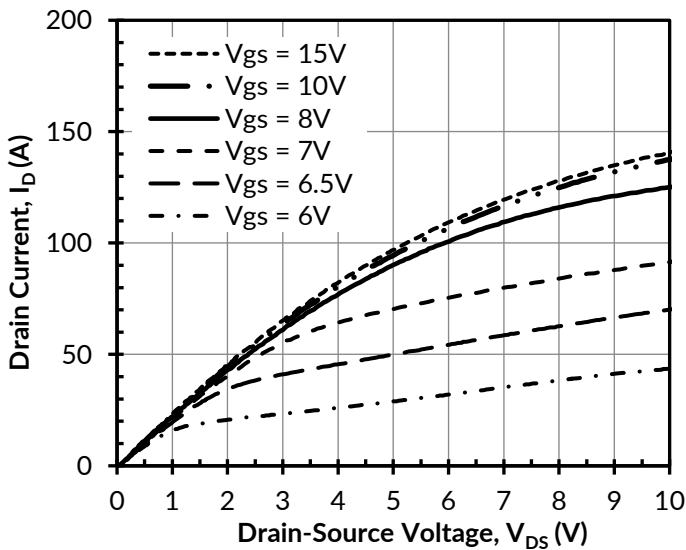


Figure 3. Typical output characteristics at $T_J = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

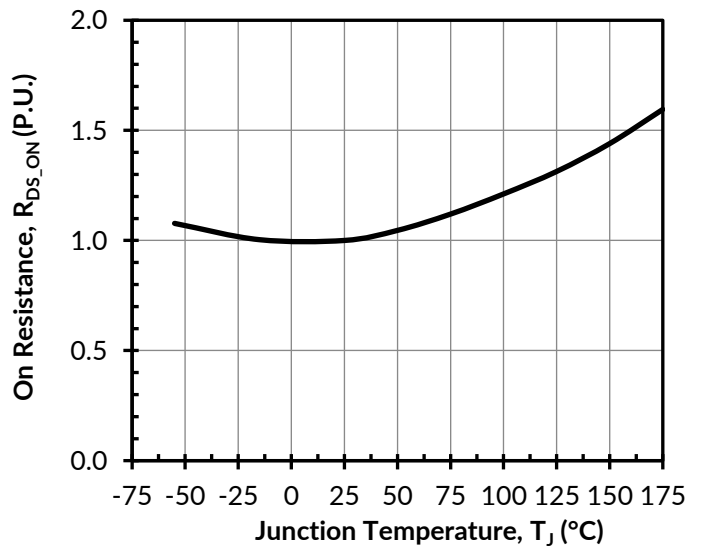


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 50\text{A}$

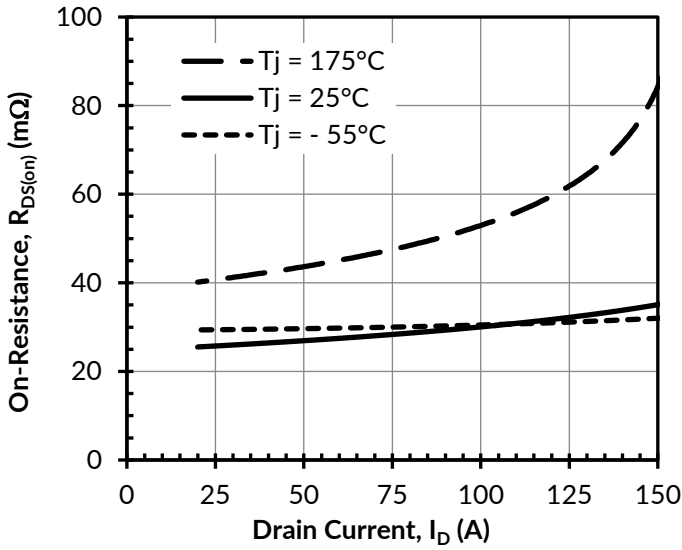


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12\text{V}$

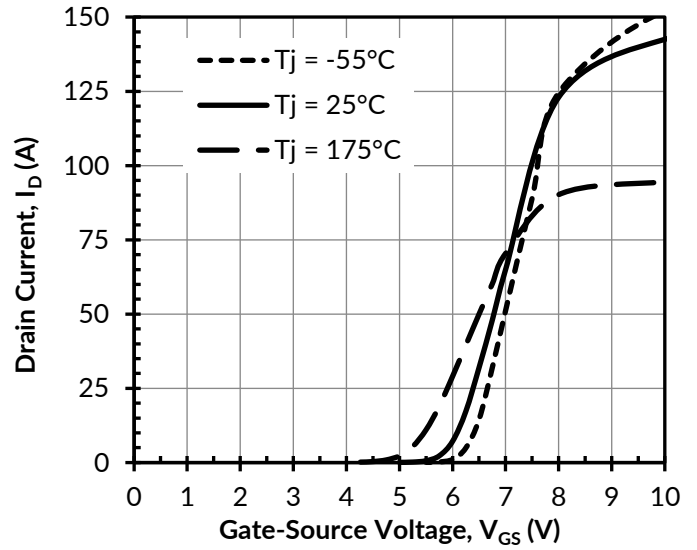


Figure 6. Typical transfer characteristics at $V_{DS} = 5\text{V}$

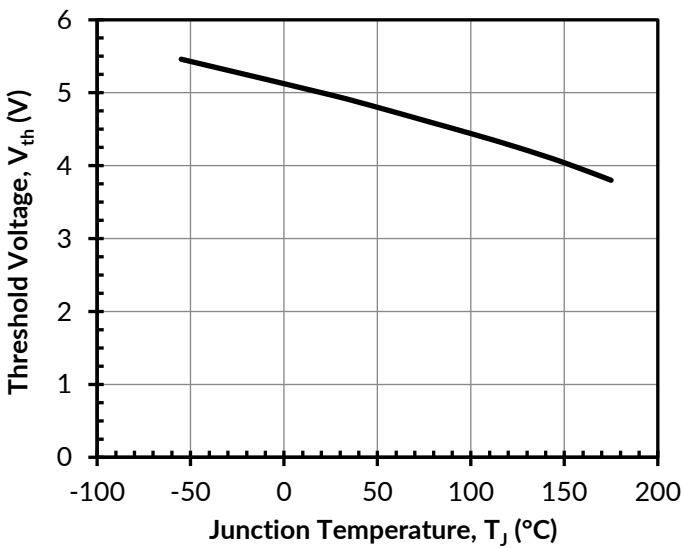


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5\text{V}$ and $I_D = 10\text{mA}$

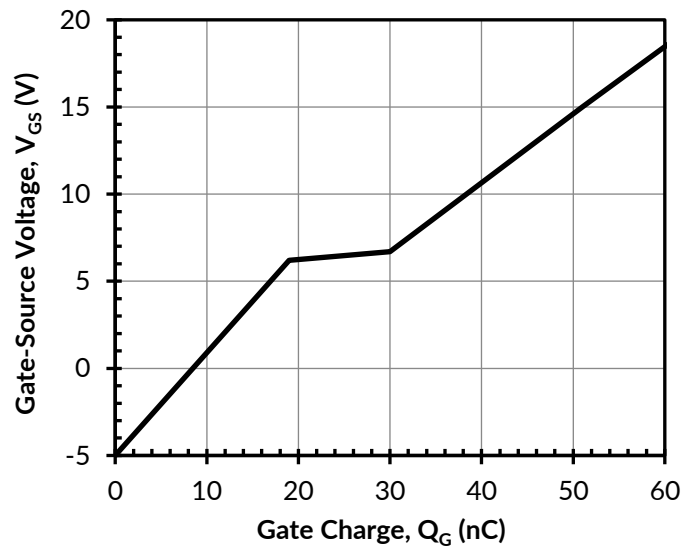


Figure 8. Typical gate charge at $V_{DS} = 400\text{V}$ and $I_D = 50\text{A}$

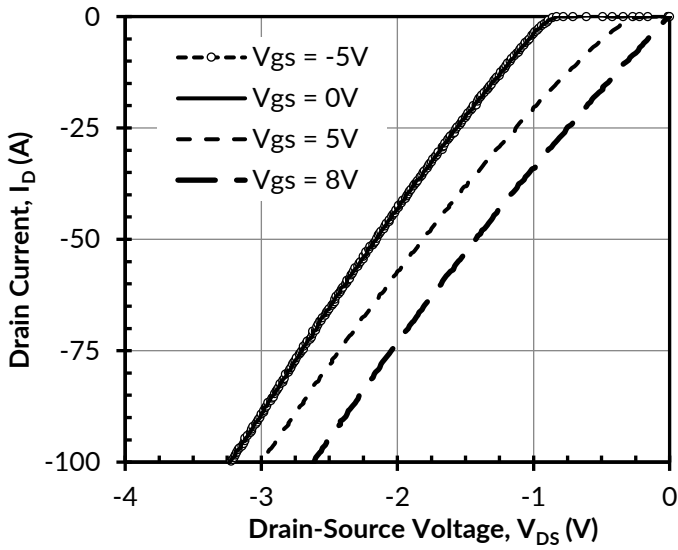


Figure 9. 3rd quadrant characteristics at $T_j = -55^\circ\text{C}$

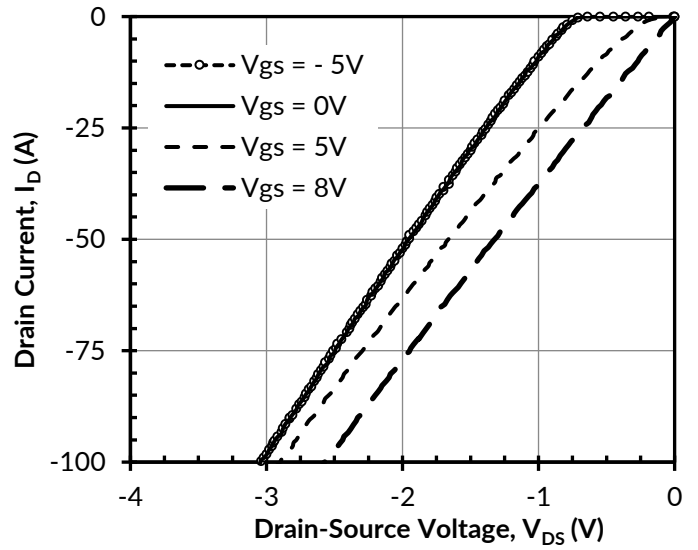


Figure 10. 3rd quadrant characteristics at $T_j = 25^\circ\text{C}$

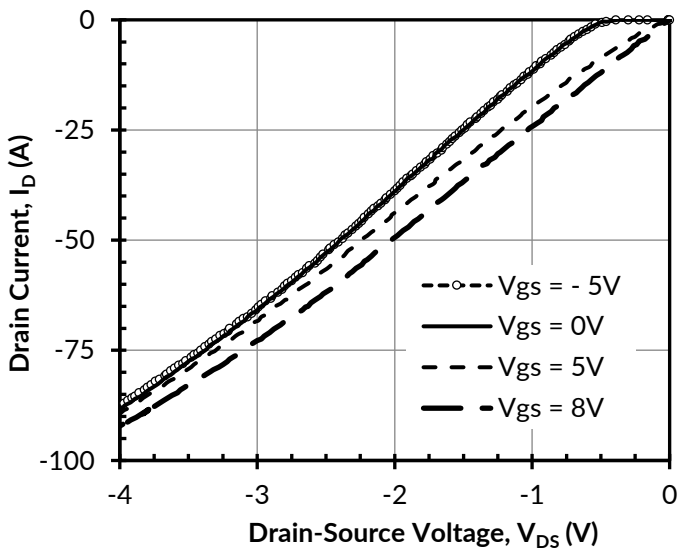


Figure 11. 3rd quadrant characteristics at $T_j = 175^\circ\text{C}$

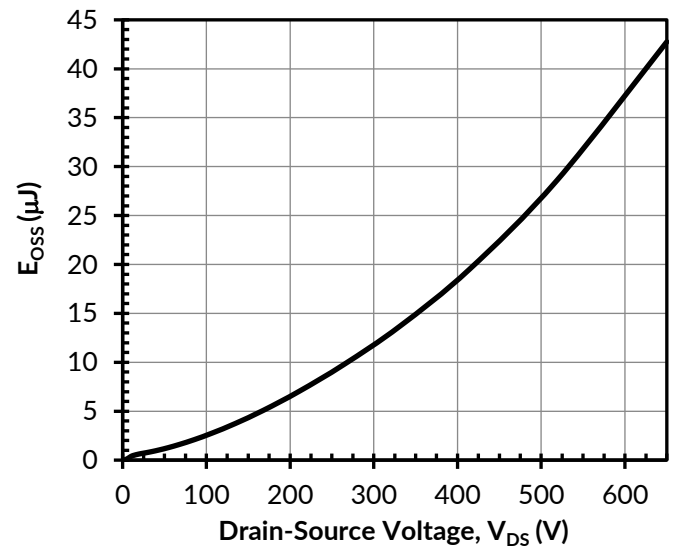


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$

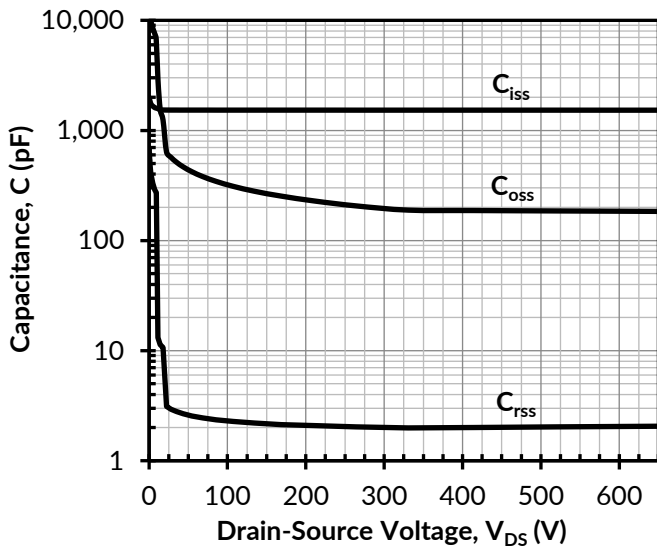


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

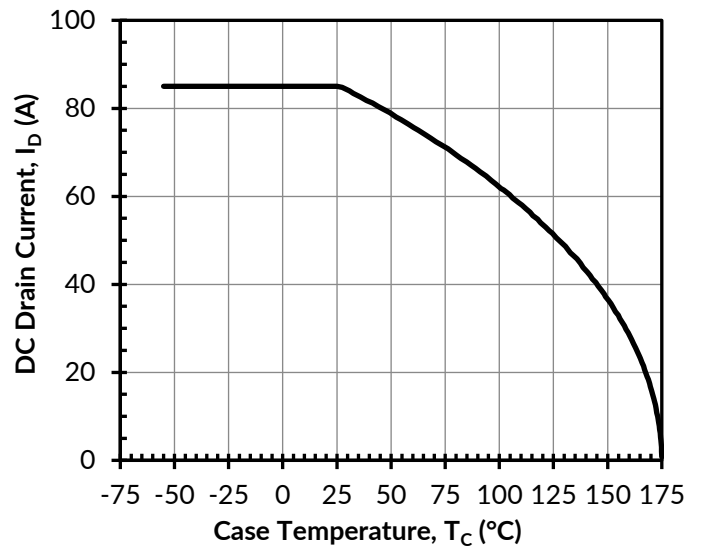


Figure 14. DC drain current derating

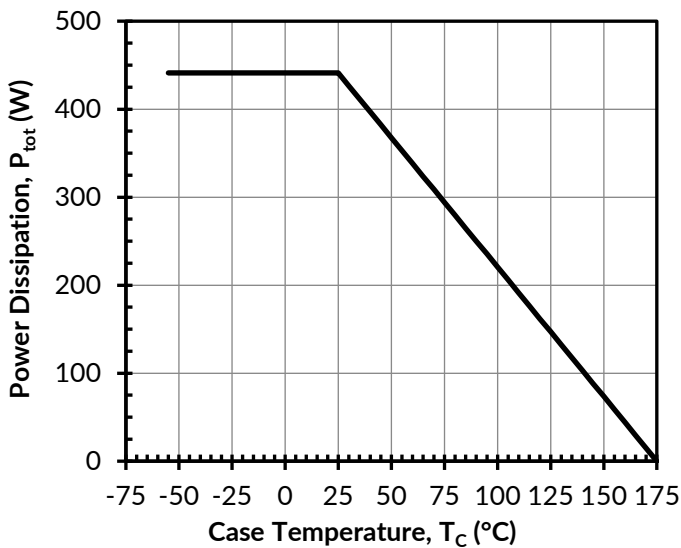


Figure 15. Total power dissipation

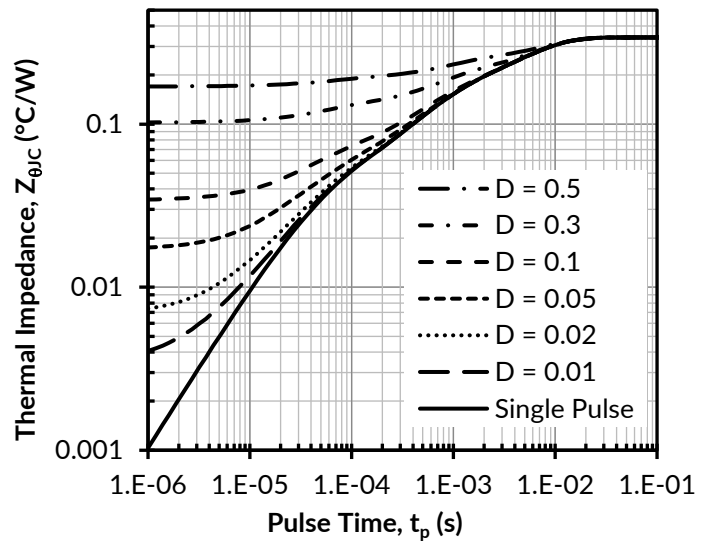


Figure 16. Maximum transient thermal impedance

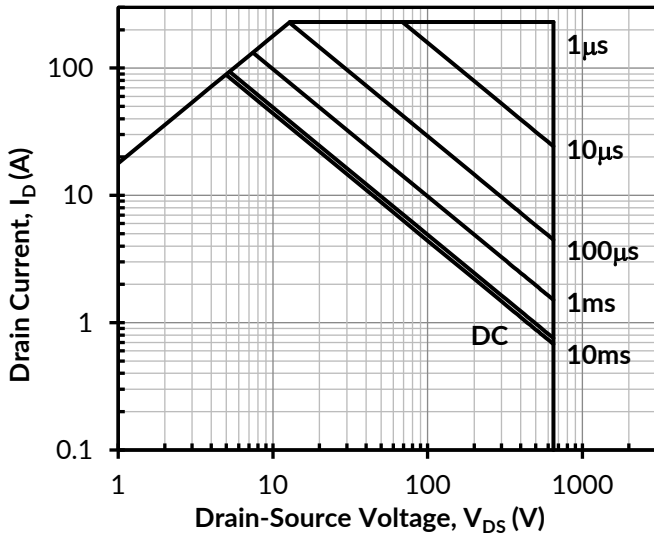


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

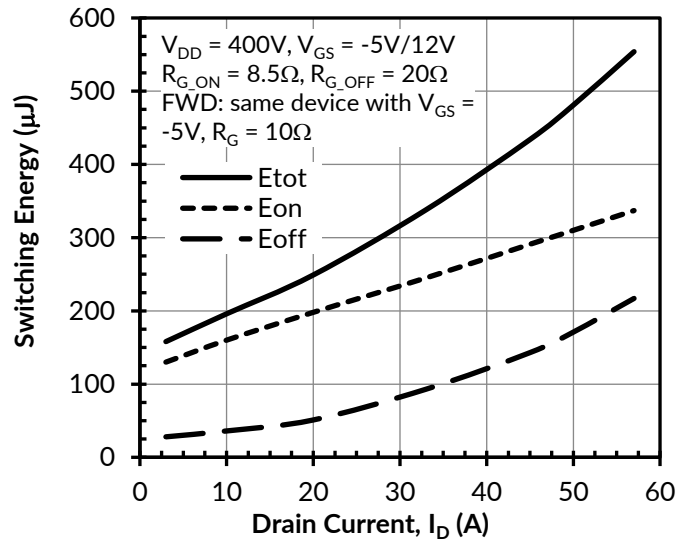


Figure 18. Clamped inductive switching energy vs. drain current at $T_J = 25^\circ\text{C}$

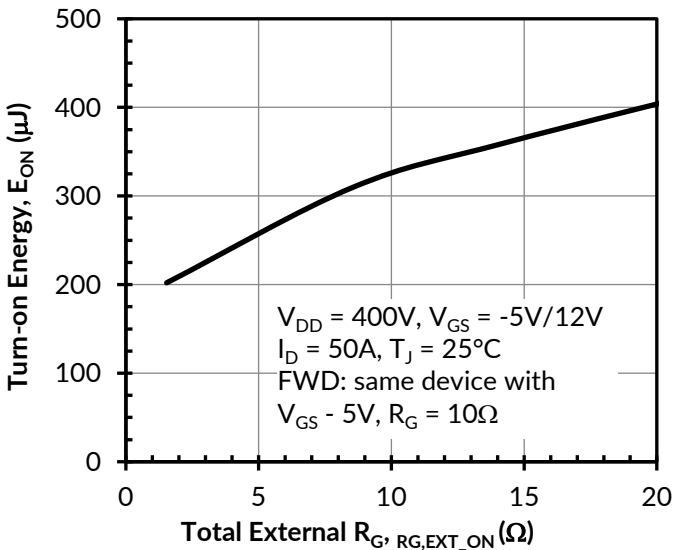


Figure 19. Clamped inductive switching turn-on energy vs. R_{G,EXT_ON}

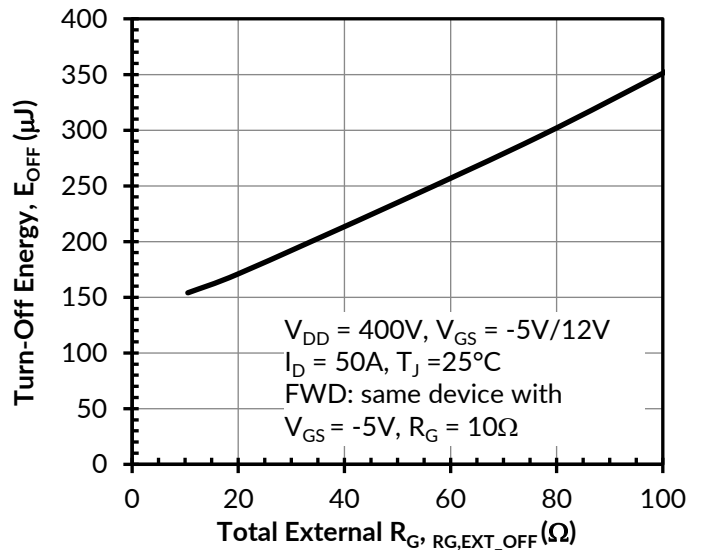


Figure 20. Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

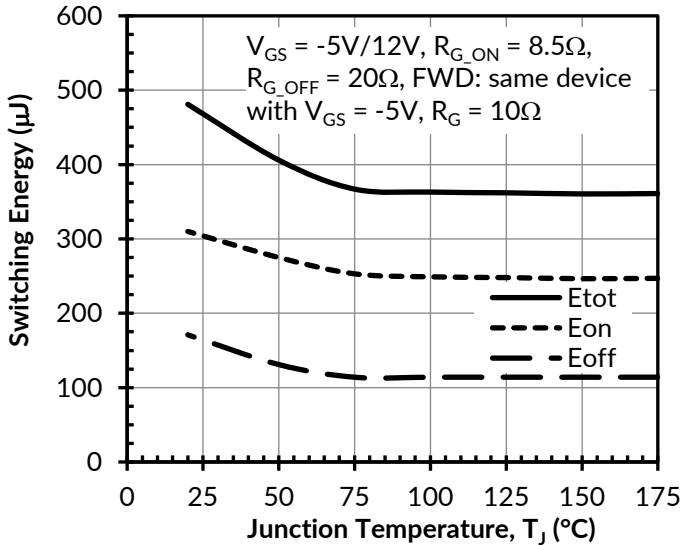


Figure 21. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 400V$ and $I_D = 50A$

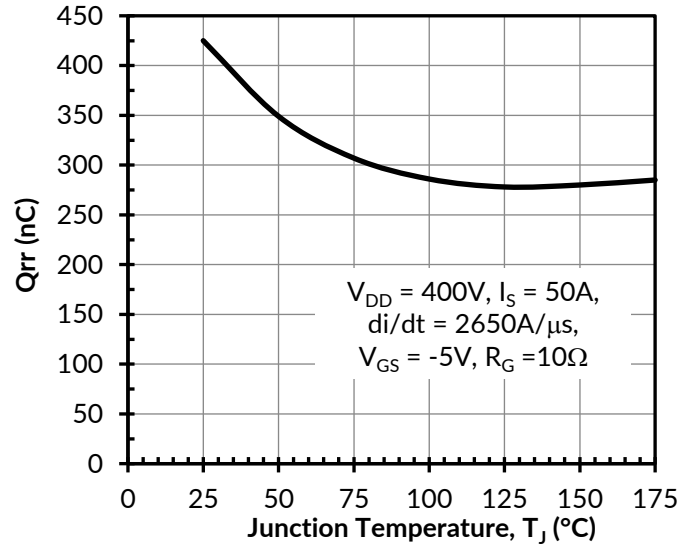


Figure 22. Reverse recovery charge Q_{rr} vs. junction temperature

Applications Information

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on cascode operation, see www.unitedsic.com.

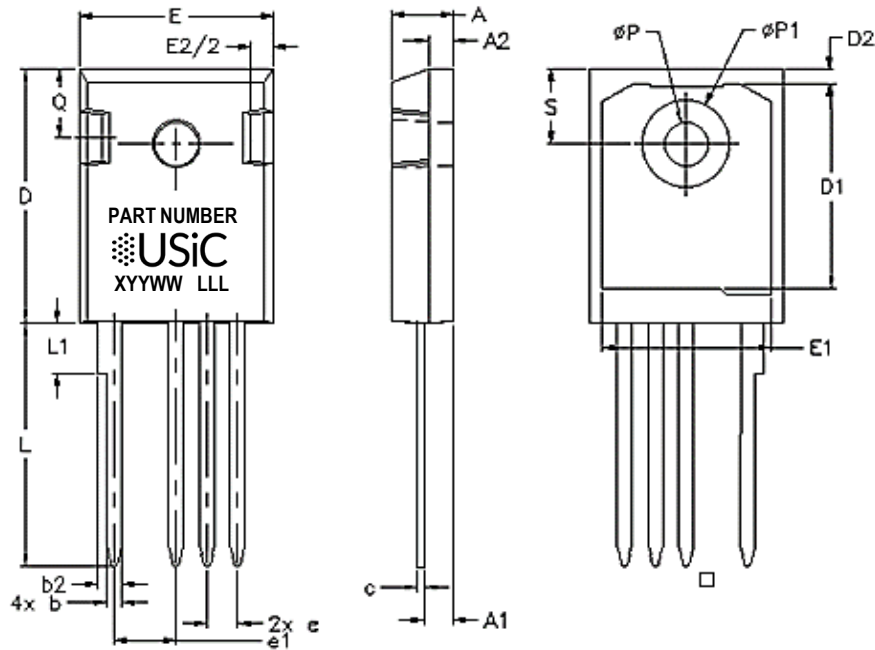
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PACKAGE OUTLINE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.185	0.209	4.7	5.31
A1	0.087	0.102	2.21	2.59
A2	0.059	0.098	1.5	2.49
b	0.039	0.055	0.99	1.4
b2	0.065	0.094	1.65	2.39
c	0.015	0.035	0.38	0.89
D	0.819	0.845	20.8	21.46
D1	0.515	-	13.08	-
D2	0.02	0.053	0.51	1.35
E	0.61	0.64	15.49	16.26
e	0.100 BSC		2.54 BSC	
e1	0.19	0.21	4.83	5.33
E1	0.53	-	13.46	-
E2	0.14	0.16	3.56	4.06
L	0.78	0.8	19.81	20.32
L1	-	0.177	-	4.5
ϕP	0.14	0.144	3.56	3.66
$\phi P1$	0.278	0.291	7.06	7.39
Q	0.212	0.244	5.38	6.2
S	0.243 BSC		6.17 BSC	



PART MARKING

TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PART NUMBER

The logo for USiC, featuring a circular pattern of black dots on the left and the text "USiC" in a large, bold, black sans-serif font on the right.
XYYWW LLL

PART NUMBER = REFER TO
DS_PN DECODER FOR DETAILS

X = ASSEMBLY SITE

YY = YEAR

WW = WORK WEEK

LLL = LOT ID

PACKING TYPE

ANTI-STATIC TUBE

QUANTITY /TUBE : 30 UNITS

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