SiC JFET Division

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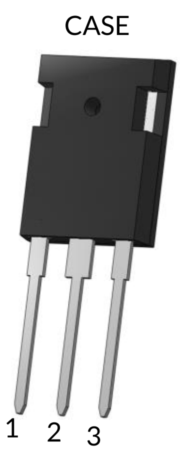
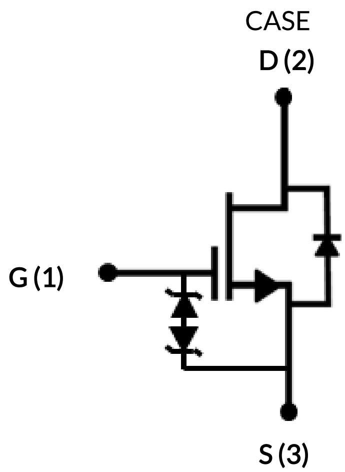
DATASHEET

UF3C065030K3S





Part Number	Package	Marking
UF3C065030K3S	TO-247-3L	UF3C065030K3S

RoHS COMPLIANT · Pb LEAD FREE · HF HALOGEN FREE · Green

Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, TO-247-3L, 650 V, 27 mohm

Rev. D, January 2025

Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-247-3L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads when used with recommended RC-snubbers, and any application requiring standard gate drive.

Features

- Typical on-resistance $R_{DS(on),typ}$ of 27mΩ
- Maximum operating temperature of 175°C
- Excellent reverse recovery
- Low gate charge
- Low intrinsic capacitance
- ESD protected, HBM class 2
- Very low switching losses (required RC-snubber loss negligible under typical operating conditions)

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current [1]	I_D	T_C = 25°C	85	A
		T_C = 100°C	62	A
Pulsed drain current [2]	I_{DM}	T_C = 25°C	230	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =4A	120	mJ
Power dissipation	P_{tot}	T_C = 25°C	441	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	°C

1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.26	0.34	°C/W

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	650			V
Total drain leakage current	I_{DSS}	V_{DS}=650V, V_{GS}=0V, T_J=25°C		6	150	μA
		V_{DS}=650V, V_{GS}=0V, T_J=175°C		30		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_J=25°C, V_{GS}=-20V / +20V		6	± 20	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=50A, T_J=25°C		27	35	mΩ
		V_{GS}=12V, I_D=50A, T_J=125°C		35		
		V_{GS}=12V, I_D=50A, T_J=175°C		43		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=10mA	4	5	6	V
Gate resistance	R_G	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C=25°C			85	A
Diode pulse current [2]	$I_{S,pulse}$	T_C=25°C			230	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_F=20A, T_J=25°C		1.3	1.4	V
		V_{GS}=0V, I_F=20A, T_J=175°C		1.35		
Reverse recovery charge	Q_{rr}	V_R=400V, I_F=50A, V_{GS}=-5V, R_{G_EXT}=20Ω di/dt=1300A/μs, T_J=25°C		218		nC
Reverse recovery time	t_{rr}			38		ns
Reverse recovery charge	Q_{rr}	V_R=400V, I_F=50A, V_{GS}=-5V, R_{G_EXT}=20Ω di/dt=1300A/μs, T_J=150°C		188		nC
Reverse recovery time	t_{rr}			35		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value Min	Value Typ	Value Max	Units
Input capacitance	C_{iss}	V_{DS}=100V, V_{GS}=0V f=100kHz		1500		pF
Output capacitance	C_{oss}			293		
Reverse transfer capacitance	C_{rss}			2		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 400V, V_{GS}=0V		215		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 400V, V_{GS}=0V		480		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=400V, V_{GS}=0V		17.5		μJ
Total gate charge	Q_G	V_{DS}=400V, I_D=50A, V_{GS} = -5V to 15V		51		nC
Gate-drain charge	Q_{GD}			11		
Gate-source charge	Q_{GS}			19		
Turn-on delay time	$t_{d(on)}$	V_{DS}=400V, I_D=50A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1.8Ω, Turn-off $R_{G,EXT}$=22Ω Inductive Load, FWD: same device with V_{GS} = -5V and R_G = 22Ω, RC snubber: R_S=5Ω and C_S=330pF, T_J=25°C		45		ns
Rise time	t_r			28		
Turn-off delay time	$t_{d(off)}$			59		
Fall time	t_f			18		
Turn-on energy including R_S energy[4]	E_{ON}			752		μJ
Turn-off energy including R_S energy[4]	E_{OFF}			178		
Total switching energy including R_S energy[4]	E_{TOTAL}			930		
Snubber R_S energy during turn-on	E_{RS_ON}			4.4		
Snubber R_S energy during turn-off	E_{RS_OFF}			11.3		
Turn-on delay time	$t_{d(on)}$	V_{DS}=400V, I_D=50A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1.8Ω, Turn-off $R_{G,EXT}$=22Ω Inductive Load, FWD: same device with V_{GS} = -5V and R_G = 22Ω, RC snubber: R_S=5Ω and C_S=330pF, T_J=150°C		43		ns
Rise time	t_r			28		
Turn-off delay time	$t_{d(off)}$			61		
Fall time	t_f			17		
Turn-on energy including R_S energy[4]	E_{ON}			704		μJ
Turn-off energy including R_S energy[4]	E_{OFF}			195		
Total switching energy including R_S energy[4]	E_{TOTAL}			899		
Snubber R_S energy during turn-on	E_{RS_ON}			4.2		
Snubber R_S energy during turn-off	E_{RS_OFF}			11.3		

4. The switching performance are evaluated with a RC snubber circuit as shown in Figure 24.

Typical Performance Diagrams

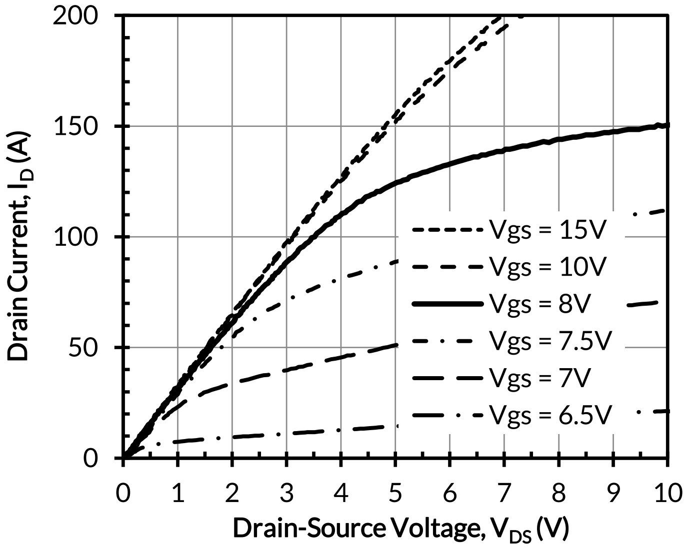


Figure 1. Typical output characteristics at T_J = - 55°C, t_p < 250µs

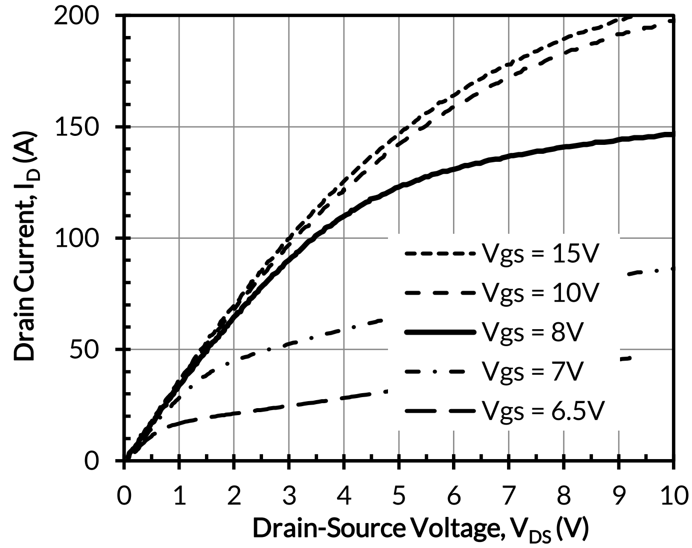


Figure 2. Typical output characteristics at T_J = 25°C, t_p < 250µs

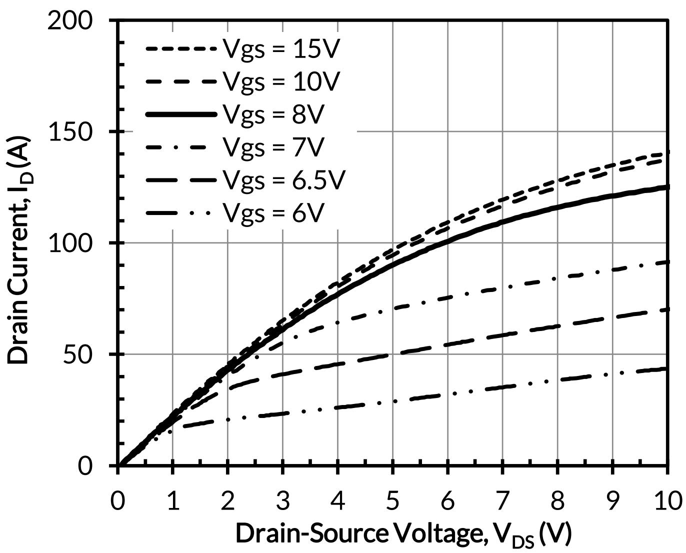


Figure 3. Typical output characteristics at T_J = 175°C, t_p < 250µs

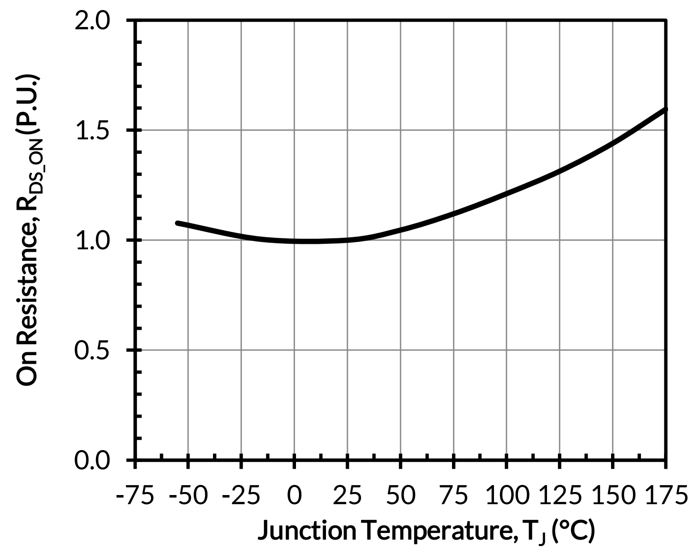


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 50A

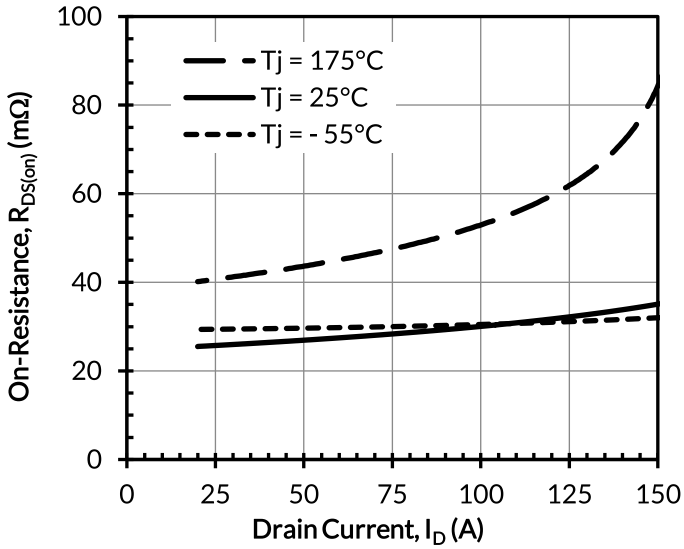


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

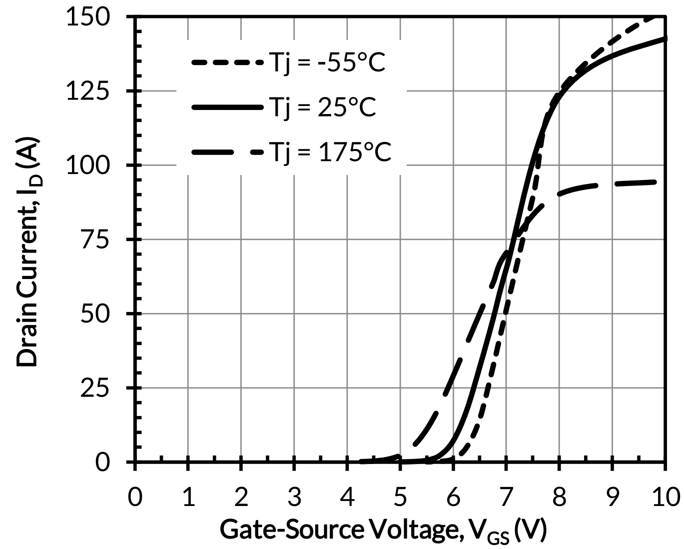


Figure 6. Typical transfer characteristics at V_{DS} = 5V

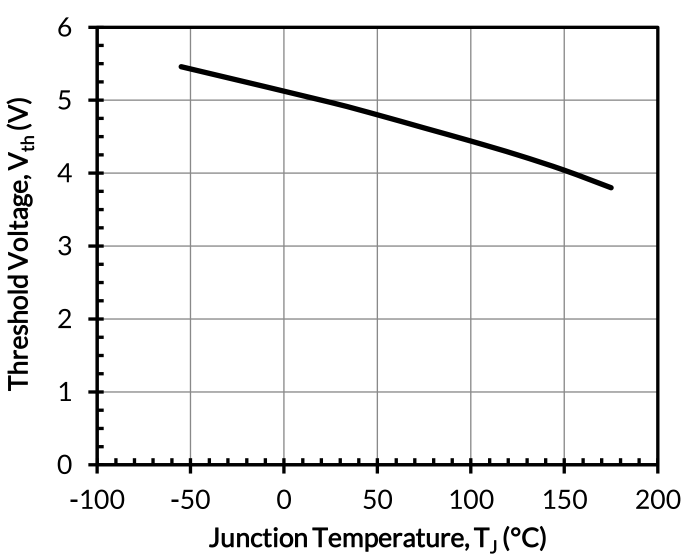


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

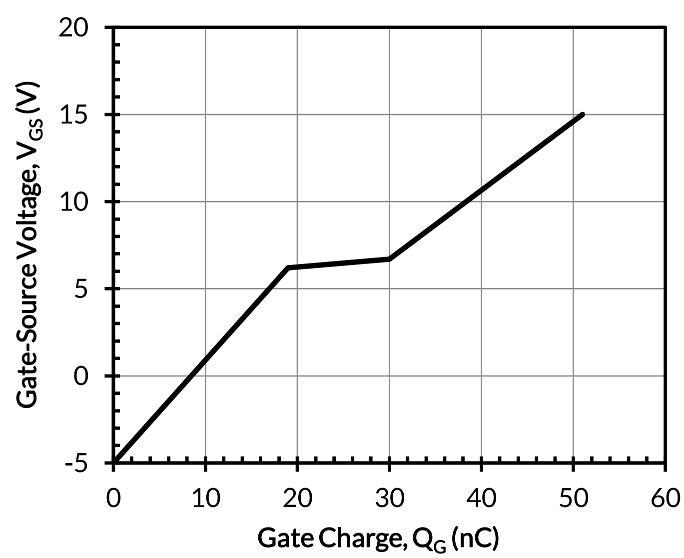


Figure 8. Typical gate charge at V_{DS} = 400V and I_D = 50A

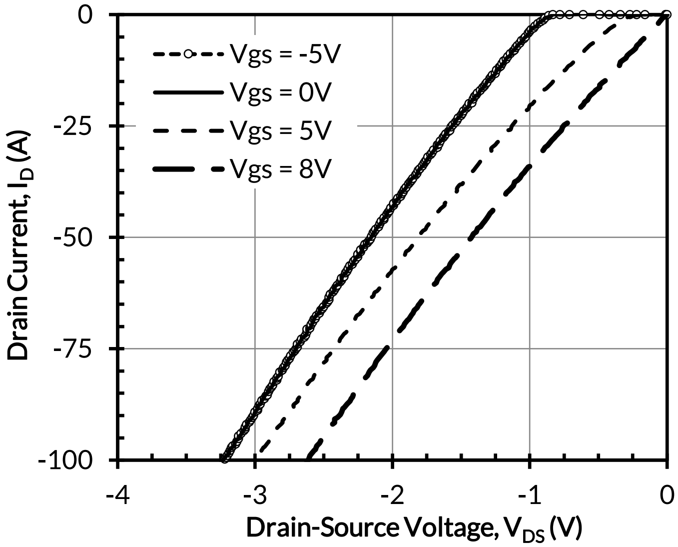


Figure 9. 3rd quadrant characteristics at T_J = -55°C

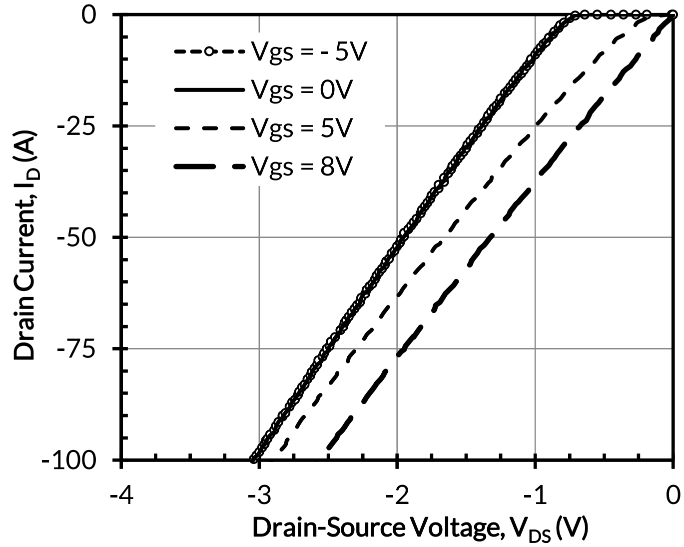


Figure 10. 3rd quadrant characteristics at T_J = 25°C

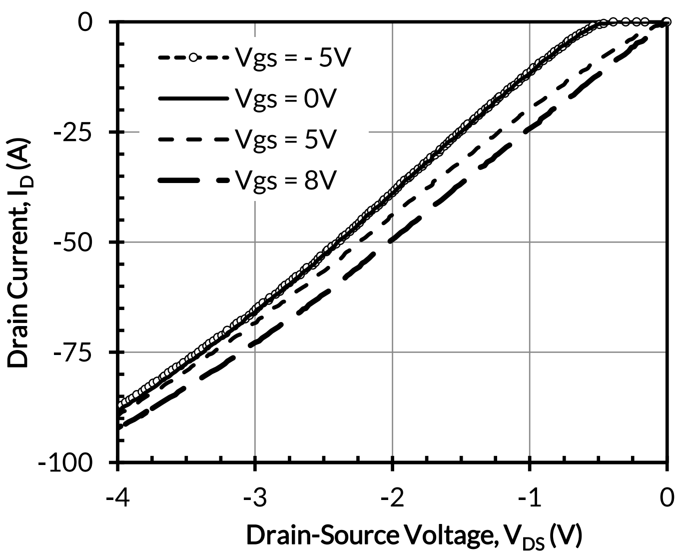


Figure 11. 3rd quadrant characteristics at T_J = 175°C

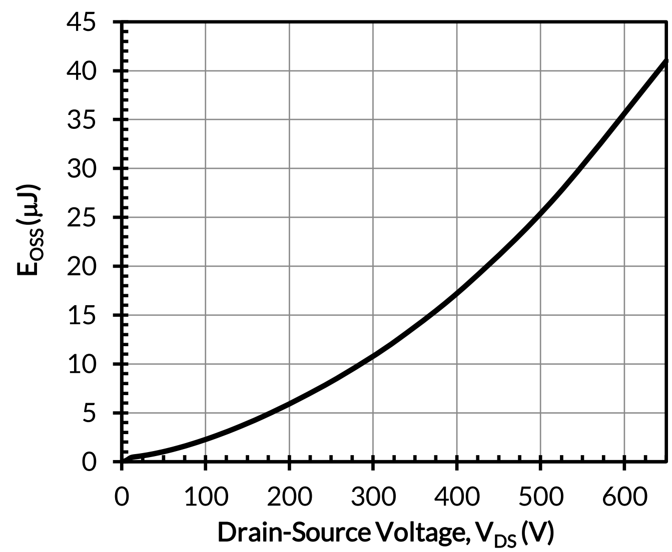


Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

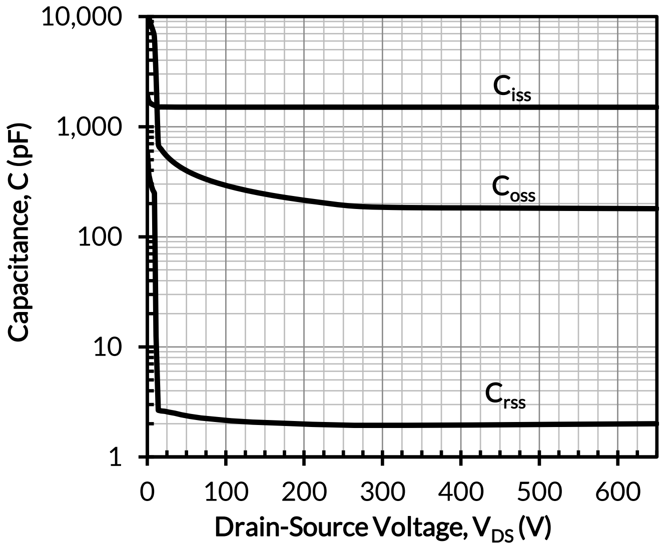


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

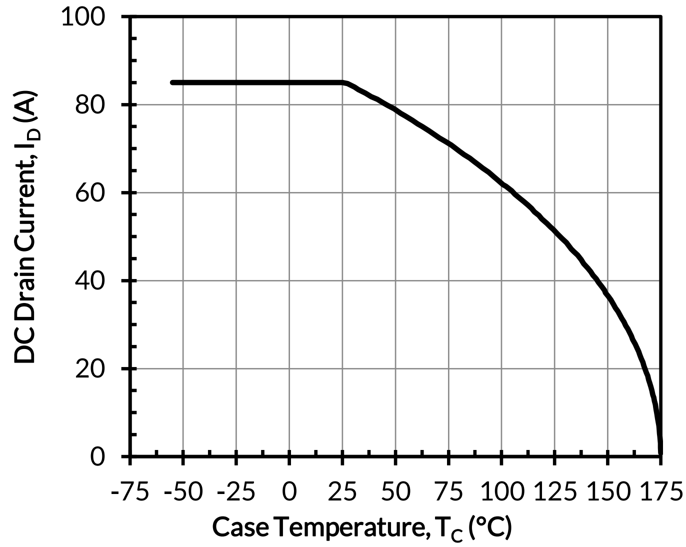


Figure 14. DC drain current derating

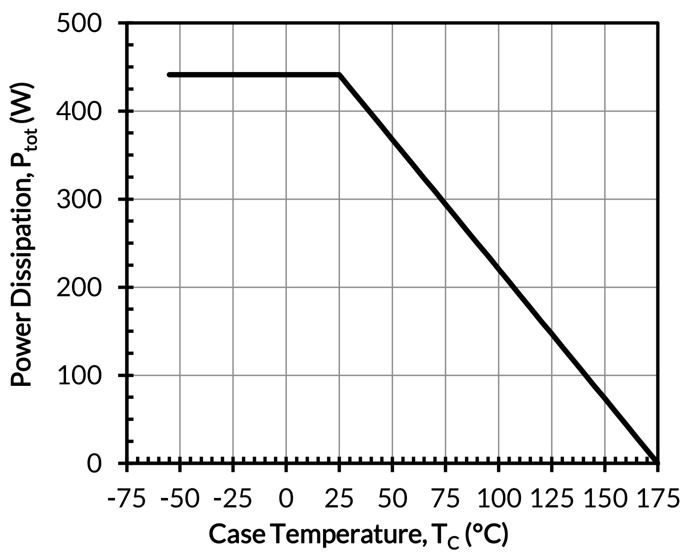


Figure 15. Total power dissipation

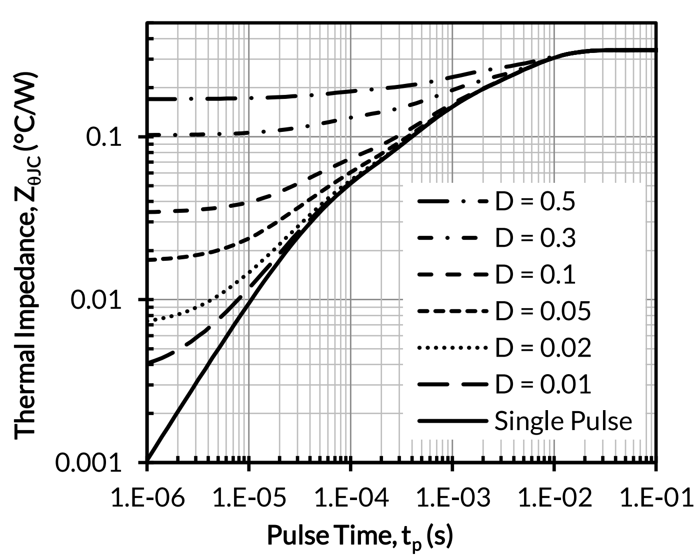


Figure 16. Maximum transient thermal impedance

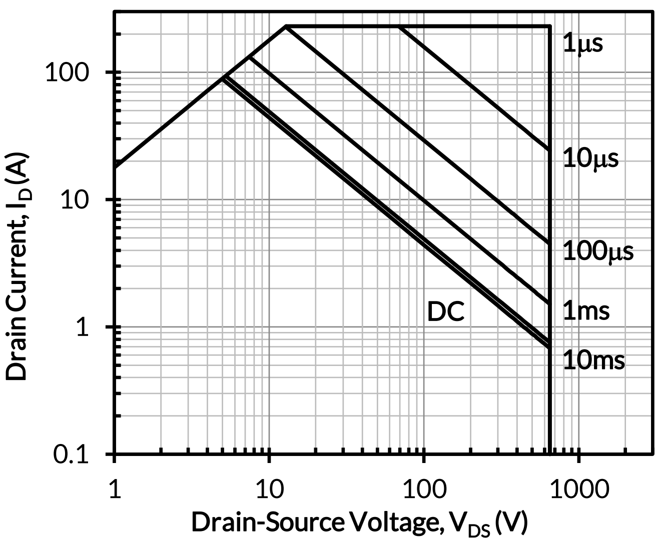


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

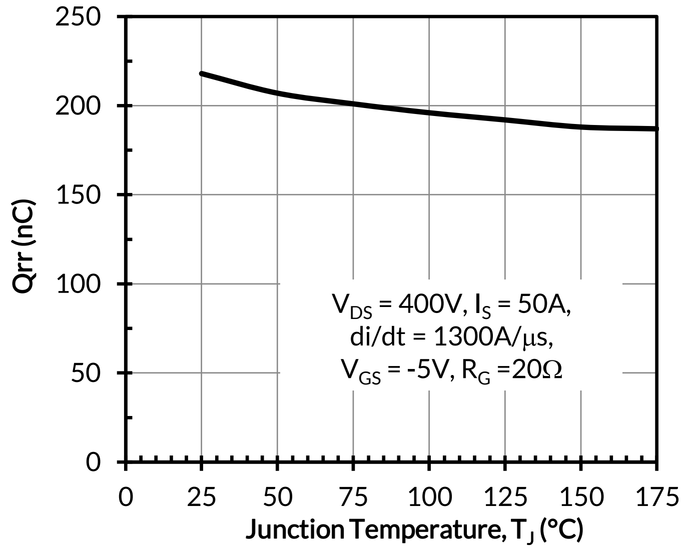
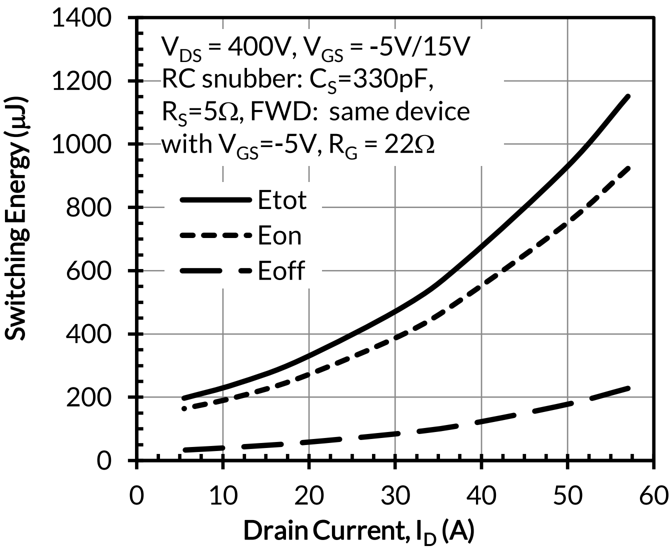
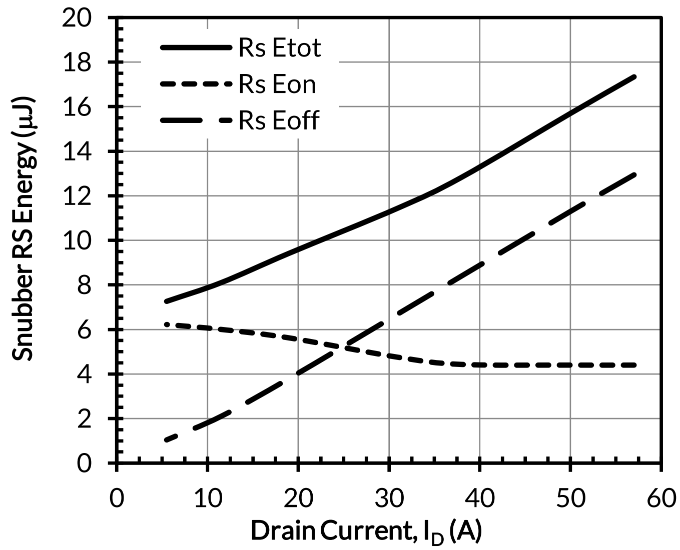


Figure 18. Reverse recovery charge Qrr vs. junction temperture



(a)



(b)

Figure 19. Clamped inductive switching energy (a) and RC snubber energy loss (b) vs. drain current at T_J = 25°C, turn-on R_{G_EXT} = 1.8Ω, and turn-off R_{G_EXT} = 22Ω

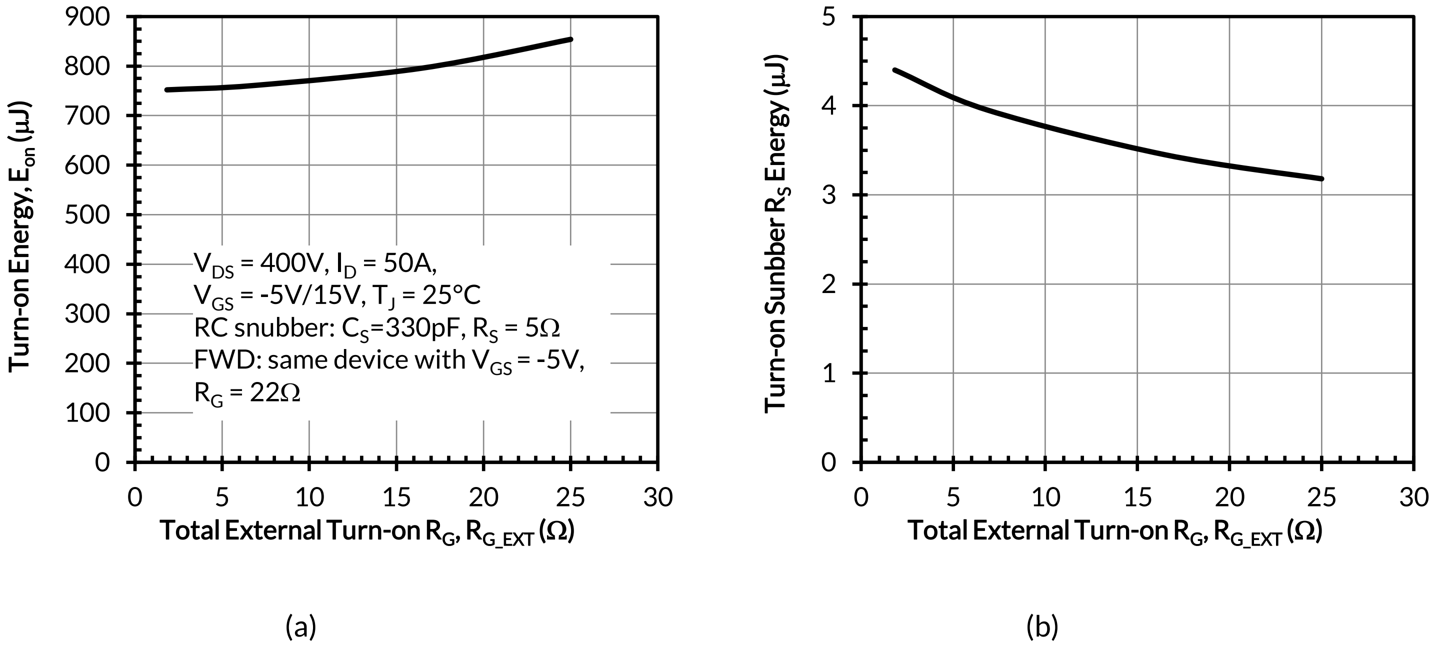


Figure 20. Clamped inductive switching turn-on energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of total external turn-on gate resistor R_{G_EXT}

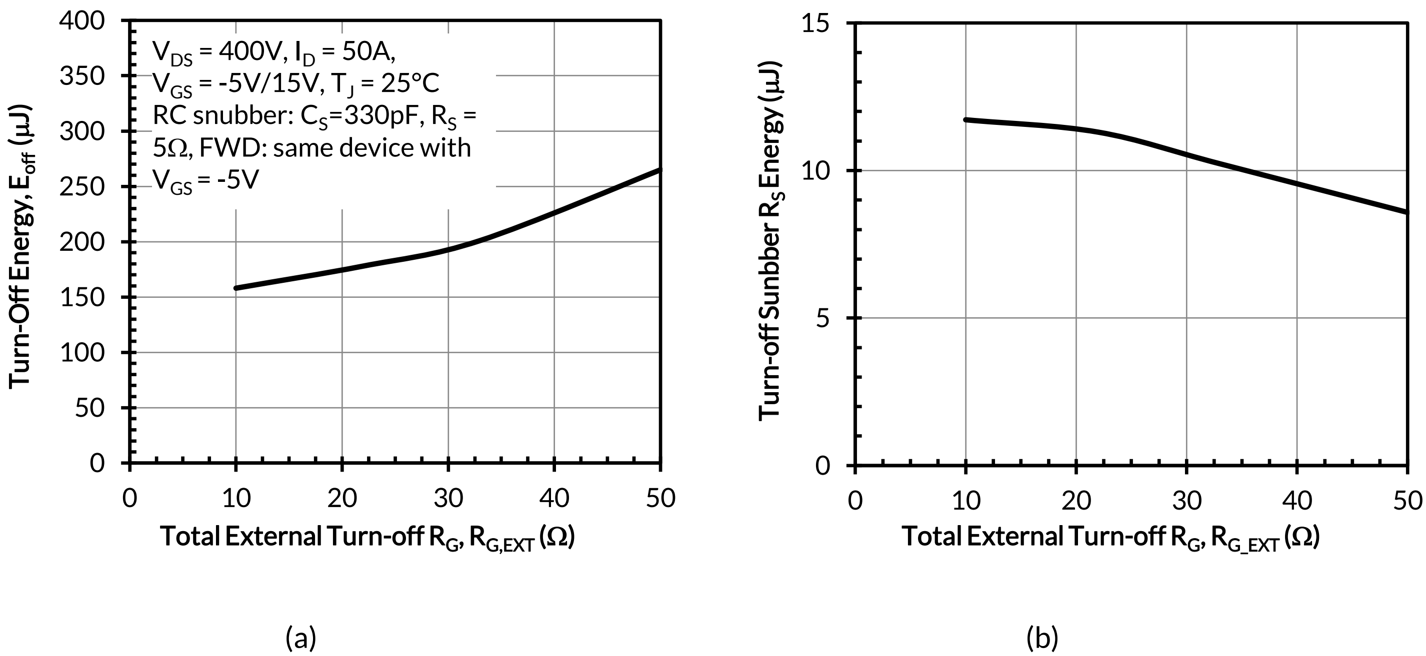
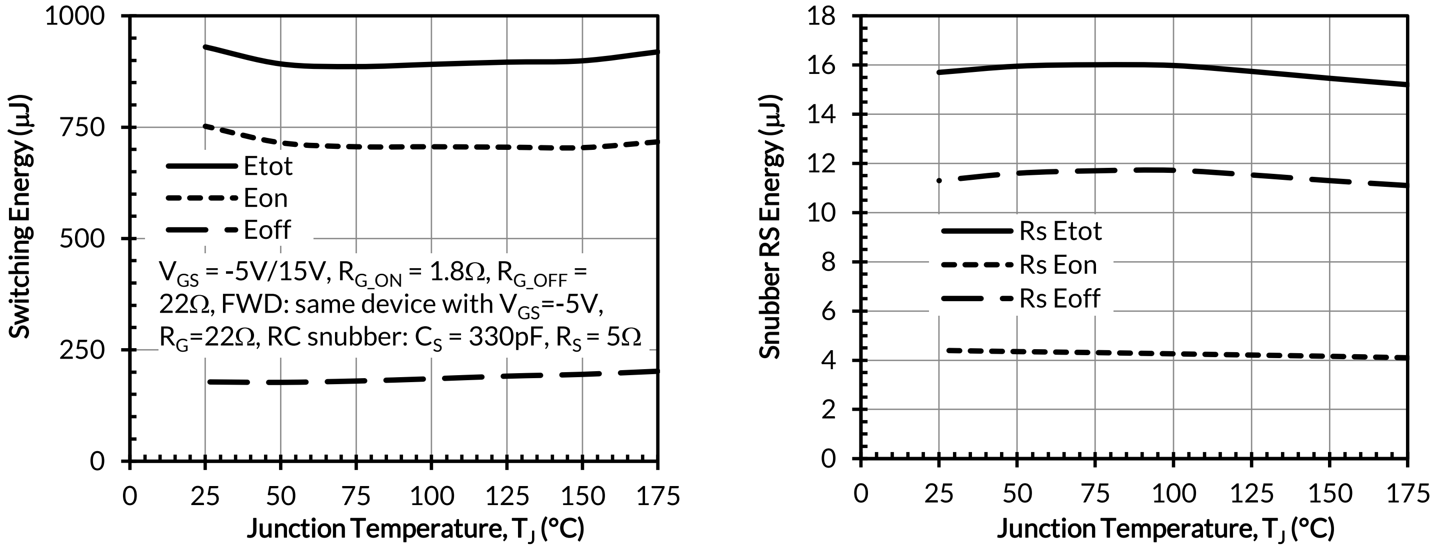
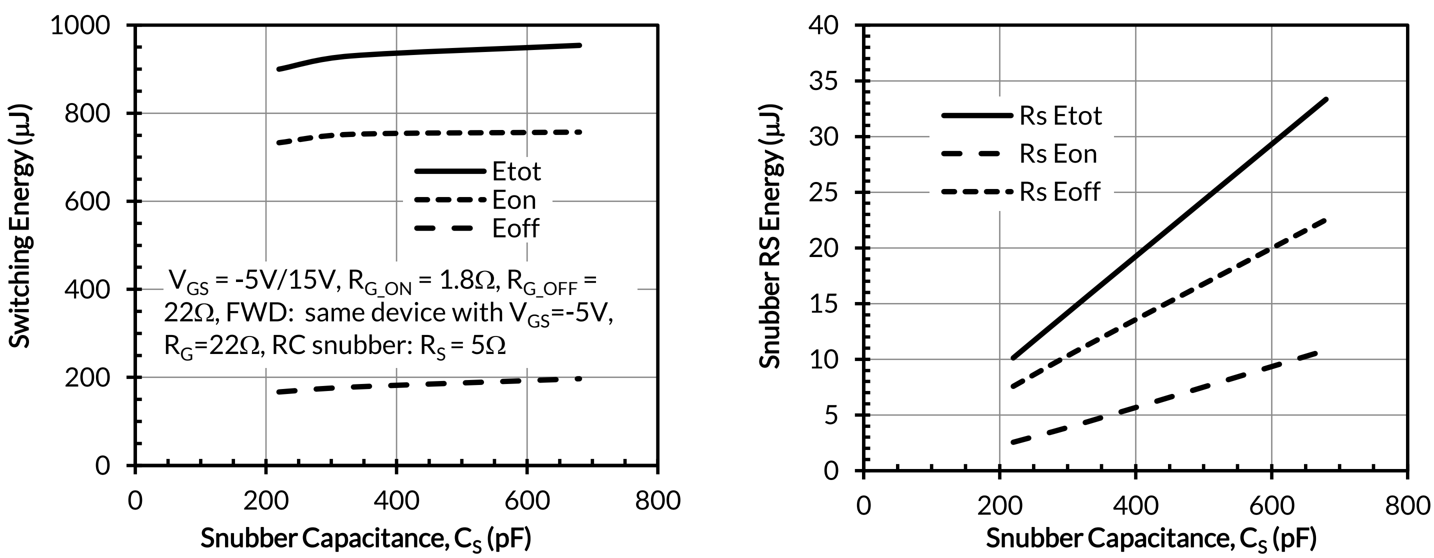


Figure 21. Clamped inductive switching turn-off energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of total external turn-off gate resistor R_{G_EXT}



(a) (b)

Figure 22. Clamped inductive switching energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of junction temperature at I_D = 50A and V_{DS} = 400V



(a) (b)

Figure 23. Clamped inductive switching energy including RC snubber energy loss (a) and RC snubber energy loss (b) as a function of snubber capacitance at I_D = 50A, V_{DS} = 400V, and T_J = 25°C

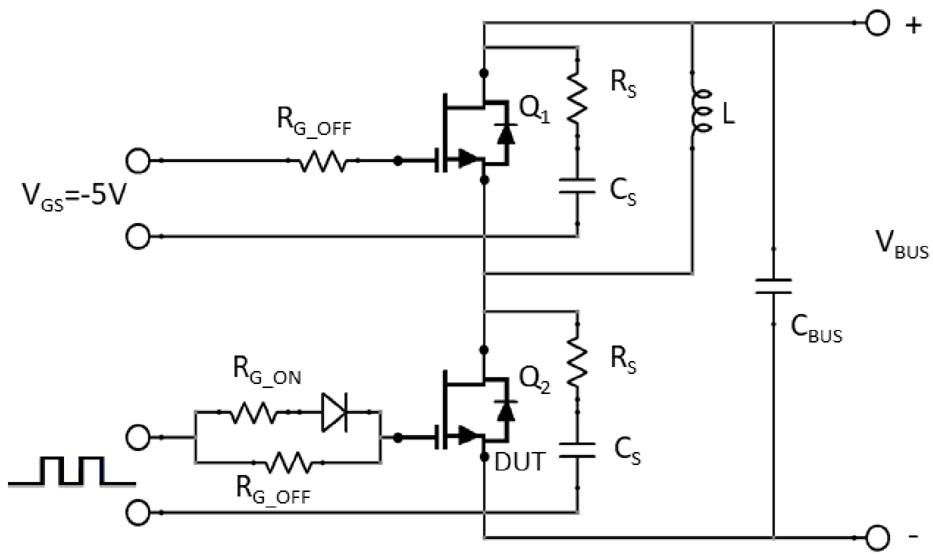


Figure 24. Clamped inductive load switching test circuit
An RC snubber (R_S = 5Ω and C_S = 330pF) is required to improve the turn-off waveforms.

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Qrr) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FEt is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

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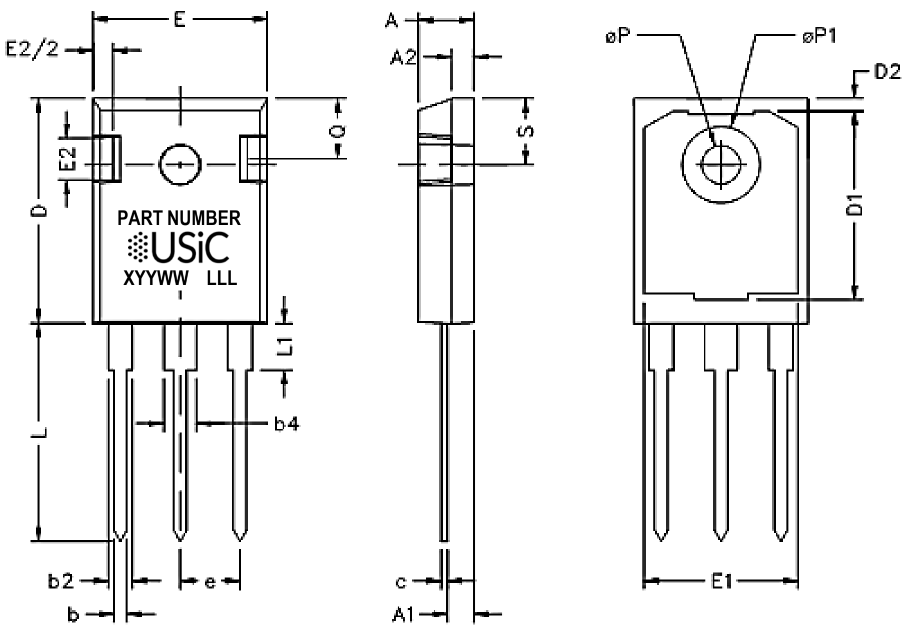
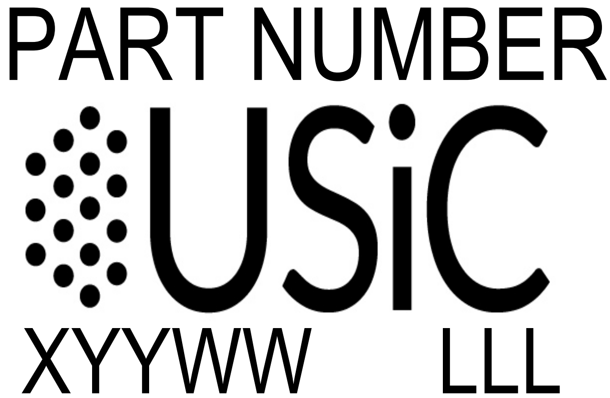


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.185	0.209	4.699	5.309
A1	0.087	0.102	2.21	2.61
A2	0.059	0.098	1.499	2.489
b	0.039	0.055	0.991	1.397
b2	0.065	0.094	1.651	2.388
b4	0.102	0.135	2.591	3.429
c	0.015	0.035	0.381	0.889
D	0.819	0.845	20.803	21.463
D1	0.515	-	13.081	-
D2	0.02	0.053	0.508	1.346
E	0.61	0.64	15.494	16.256
e	0.214 BSC		5.44 BSC	
E1	0.53	-	13.462	-
E2	0.135	0.157	3.429	3.988
L	0.78	0.8	19.812	20.32
L1	-	0.177	-	4.496
ØP	0.14	0.144	3.556	3.658
ØP1	0.278	0.291	7.061	7.391
Q	0.212	0.244	5.385	6.198
S	0.243 BSC		6.17 BSC	

TO-247-3L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PART MARKING



PART NUMBER = REFER TO DS_PN DECODER FOR DETAILS

X = ASSEMBLY SITE
YY = YEAR
WW = WORK WEEK
LLL = LOT ID

PACKING TYPE

ANTI-STATIC TUBE

QUANTITY /TUBE : 30 UNITS

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