Low-Voltage Multiplexer/Demultiplexer, Bus Switch

Product Preview

T30LMSW3B3257 / T30LMSW3B3253 / T30LMSW3B3125 / T30LMSW3B3126

The T30LMSW3B3257 device is a 4-bit 1-of-2 highspeed FET multiplexer/demultiplexer. The select (S) input controls the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable ($\overline{OE}$) input is high.

The T30LMSW3B3253 device is a dual 1-of-4 highspeed FET multiplexer and demultiplexer. The select (S0, S1) inputs control the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable ($\overline{OE}$) input is high.

The T30LMSW3B3125 and T30LMSW3B3126 devices are quadruple FET bus switches featuring independent line switches. Each switch of the T30LMSW3B3125 is disabled when the associated output-enable ($\overline{OE}$) input is high. Each switch of the T30LMSW3B3126 is disabled when the associated output-enable (OE) input is low.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the devices when the devices are powered down. The devices have isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor while OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Features

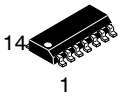
- 5 Ω Switch Connection Between 2 Ports
- Rail to Rail Switching on Data Ports
- I_{off} Supports Partial Power Down Mode Operation
- Break-Before-Make circuitry for 3257 and 3253
- 2000 V HBM ESD Protection (JESD22)

Typical Applications

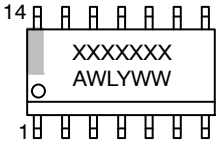
- Internet of Things
- Wireless Headphones
- Muxing/Demuxing
- Datacenters and Enterprise Computing
- Building Automation

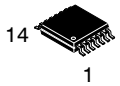
This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

MARKING DIAGRAMS

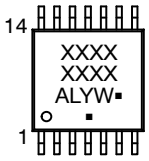


SOIC-14
D SUFFIX
CASE 751A

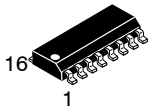




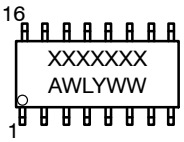
TSSOP-14
DT SUFFIX
CASE 948G

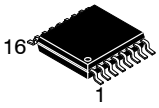


SSOP-14
DS SUFFIX
CASE TBD



SOIC-16
D SUFFIX
CASE 751B





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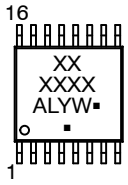
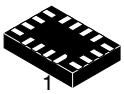
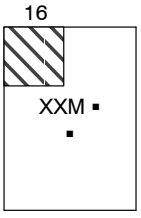
DT SUFFIX
CASE 948F



SSOP-16
DS SUFFIX
CASE TBD



UQFN16
MU2 SUFFIX
1.8x2.6, 0.4P
CASE 488AU



XXXXXX	= Specific Device Code
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

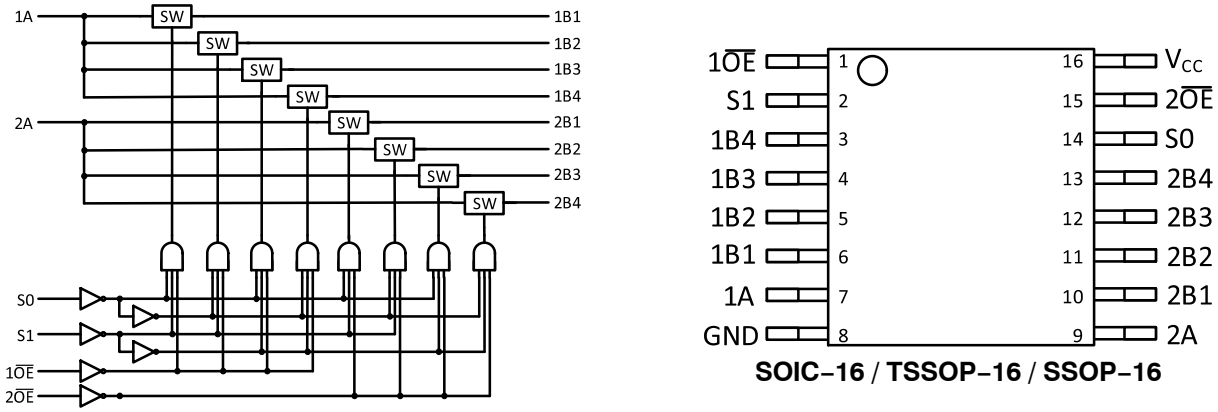


Figure 1. T30LMSW3B3253 Logic Diagram and Pin Assignment

T30LMSW3B3253 FUNCTION TABLE

Inputs			Function
$\overline{OE}$	S1	S0	
L	L	L	A = B1
L	L	H	A = B2
L	H	L	A = B3
L	H	H	A = B4
H	X	X	Disconnect

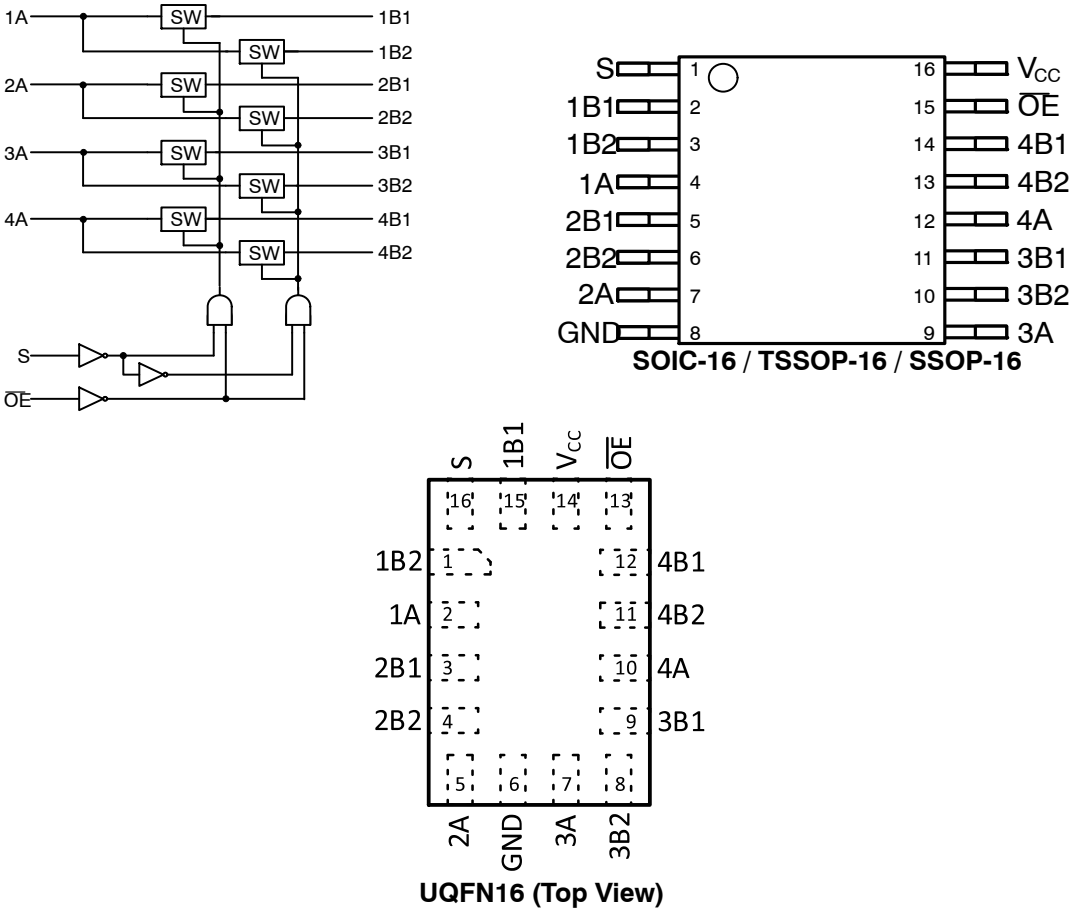


Figure 2. T30LMSW3B3257 Logic Diagram and Pin Assignment

T30LMSW3B3257 FUNCTION TABLE

Inputs		Function
$\overline{OE}$	S	
L	L	A = B1
L	H	A = B2
H	X	Disconnect

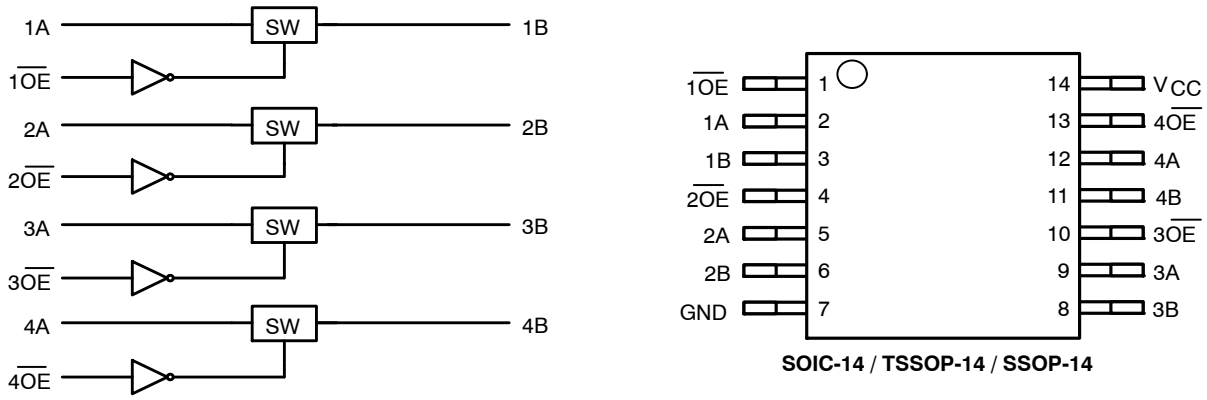
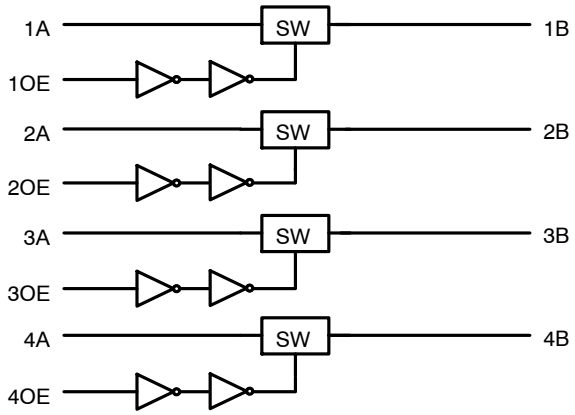
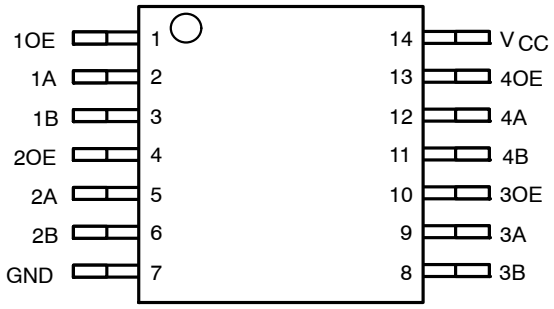


Figure 3. T30LMSW3B3125 Logic Diagram and Pin Assignment

T30LMSW3B3125 FUNCTION TABLE

$\overline{OE}$	Function
L	A = B
H	Disconnect





SOIC-14 / TSSOP-14 / SSOP-14

Figure 4. T30LMSW3B3126 Logic Diagram and Pin Assignment

T30LMSW3B3126 FUNCTION TABLE

OE	Function
L	Disconnect
H	A = B

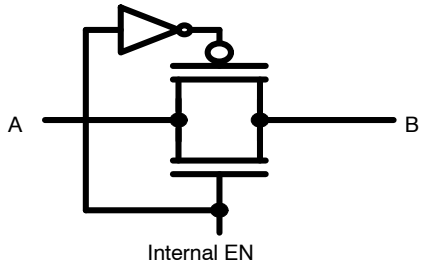


Figure 5. Individual FET Switch Simplified Schematic

MAXIMUM RATINGS

Symbol	Parameter		Condition	Value	Unit
V_{CCA}, V_{CCB}	Supply Voltage			−0.5 to +4.3	V
V_I	Input Voltage (Note 1)			−0.5 to +4.3	V
	Continuous Channel Current			128	mA
I_{IK}	Input Clamp Current		$V_{I/O}$ < GND	−50	mA
I_{CC}	DC Supply Current Per Supply Pin			±100	mA
I_{GND}	DC Ground Current per Ground Pin			±100	mA
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature			−65 to +150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC-16 SSOP-16 TSSOP16 SOIC-14 SSOP-14 TSSOP-14 UQFN16		126 TBD 159 116 TBD 150 TBD	°C/W
P_D	Power Dissipation in Still Air	SOIC-16 SSOP-16 TSSOP16 SOIC-14 SSOP-14 TSSOP-14 UQFN16		995 TBD 787 1077 TBD 833 TBD	mW
MSL	Moisture Sensitivity			Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34		UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model		2 TBD	kV
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 25 °C (Note 4)			±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CCA}, V_{CCB}	Positive DC Supply Voltage	1.65	3.6	V
V_I	Control Pin Input Voltage	GND	3.6	V
$V_{I/O}$	I/O Pin Voltage	GND	V_{CCA}	V
T_A	Operating Temperature Range	−40	+125	°C
$\Delta t/\Delta V$	Control Input Transition Rise or Fall Rate	0	200	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CCA} (V)	T_A = −40 °C to +85 °C			T_A = −40 °C to +125 °C		Unit
				Min	Typ (Note 5)	Max	Min	Max	
V_{IH}	Input HIGH Voltage		1.65–1.95	0.7 * V_{CC}	–	–	0.7 * V_{CC}	–	V
			2.3–2.7	1.7	–	–	1.7	–	
			2.7–3.6	2.0	–	–	2.0	–	
V_{IL}	Input LOW Voltage		1.65–1.95	–	–	0.3 * V_{CC}	–	0.3 * V_{CC}	V
			2.3–2.7	–	–	0.7	–	0.7	
			2.7–3.6	–	–	0.8	–	0.8	
V_{IK}	Clamp Diode Voltage	I_I = −18 mA	3.0	–	–	−1.2	–	−1.2	V
I_I	Input Leakage	V_I = V_{CC} or GND	3.6	–	–	±0.5	–	±0.5	μA
I_{off}	Power Off Leakage	V_I or V_O = GND to 3.6 V	0	–	–	1.0	–	1.0	μA
I_{CC}	Supply Current	V_I = V_{CC} or GND, I_O = 0	3.6	–	–	1.0	–	1.0	μA
ΔI_{CC}	Additional Supply Current	Control Pins; One input at 3 V, Other inputs at V_{CC} or GND	3.6	–	–	100	–	100	μA
C_I	Control Input Capacitance	V_I = 3 V or GND		–	3	–	–	–	pF
$C_{IO(off)}$	Switch Off Capacitance (T30LMSW3B3257)	$\overline{OE}$ = V_{CC}; A		–	10.5	–	–	–	pF
		V_I = 3 V or GND B		–	5.5	–	–	–	
	Switch Off Capacitance (T30LMSW3B3253)	$\overline{OE}$ = V_{CC}; A		–	20.5	–	–	–	
		V_I = 3 V or GND B		–	5.5	–	–	–	
	Switch Off Capacitance (T30LMSW3B3125 / T30LMSW3B3126)	$\overline{OE}$ = V_{CC} or OE = GND;		–	7.0	–	–	–	
		V_I = 3 V or GND							
R_{ON}	ON Resistance	V_I = 0 V; I_I = 24 mA	1.65–1.95	–	6	10	–	10	Ω
		V_I = 1.05 V; I_I = 15 mA		–	26	50	–	50	
		V_I = 0 V; I_I = 64 mA	2.3–2.7	–	4	7	–	7	
		I_I = 24 mA		–	4	7	–	7	
		V_I = 1.7 V; I_I = 15 mA		–	10	20	–	20	
		V_I = 0 V; I_I = 64 mA	3.0–3.6	–	4	6	–	6	
		I_I = 24 mA		–	4	6	–	6	
		V_I = 2.4 V; I_I = 15 mA		–	8	12	–	12	

5. All typical values are at nominal value of V_{CC} range and T_A = 25 °C.

AC ELECTRICAL CHARACTERISTICS (T30LMSW3B3257/T30LMSW3B3253)

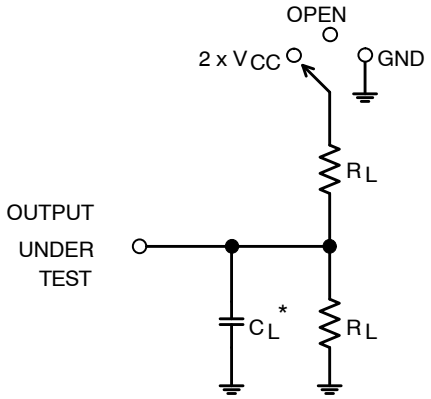
Symbol	Parameter	Test Conditions	V_{CCA} (V)	T_A = −40 °C to +85 °C			T_A = −40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	
t_{PD}	Propagation Delay (Note 6) A to B or B to A		1.65–1.95	–	–	0.15	–	0.15	ns
			2.3–2.7	–	–	0.15	–	0.15	
			2.7–3.6	–	–	0.25	–	0.25	
t_{EN}	Enable Time S to A or B		1.65–1.95	–	–	8.8	–	8.8	ns
			2.3–2.7	–	–	6.1	–	6.1	
			2.7–3.6	–	–	5.3	–	5.3	
	Enable Time $\overline{OE}$ to A or B		1.65–1.95	–	–	8.6	–	8.6	
			2.3–2.7	–	–	5.6	–	5.6	
			2.7–3.6	–	–	5	–	5	
t_{DIS}	Disable Time S to A or B		1.65–1.95	–	–	5.5	–	5.5	ns
			2.3–2.7	–	–	4.8	–	4.8	
			2.7–3.6	–	–	4.5	–	4.5	
	Disable Time $\overline{OE}$ to A or B		1.65–1.95	–	–	6.5	–	6.5	
			2.3–2.7	–	–	5.5	–	5.5	
			2.7–3.6	–	–	5.5	–	5.5	

AC ELECTRICAL CHARACTERISTICS (T30LMSW3B3125 / T30LMSW3B3126)

Symbol	Parameter	Test Conditions	V_{CCA} (V)	T_A = −40 °C to +85 °C			T_A = −40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	
t_{PD}	Propagation Delay (Note 6) A to B or B to A		1.65–1.95	–	–	0.15	–	0.15	ns
			2.3–2.7	–	–	0.15	–	0.15	
			2.7–3.6	–	–	0.25	–	0.25	
t_{EN}	Enable Time $\overline{OE}$ to A or B		1.65–1.95	–	–	8.6	–	8.6	ns
			2.3–2.7	–	–	5.6	–	5.6	
			2.7–3.6	–	–	5	–	5	
t_{DIS}	Disable Time $\overline{OE}$ to A or B		1.65–1.95	–	–	6.5	–	6.5	ns
			2.3–2.7	–	–	5.5	–	5.5	
			2.7–3.6	–	–	5.5	–	5	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

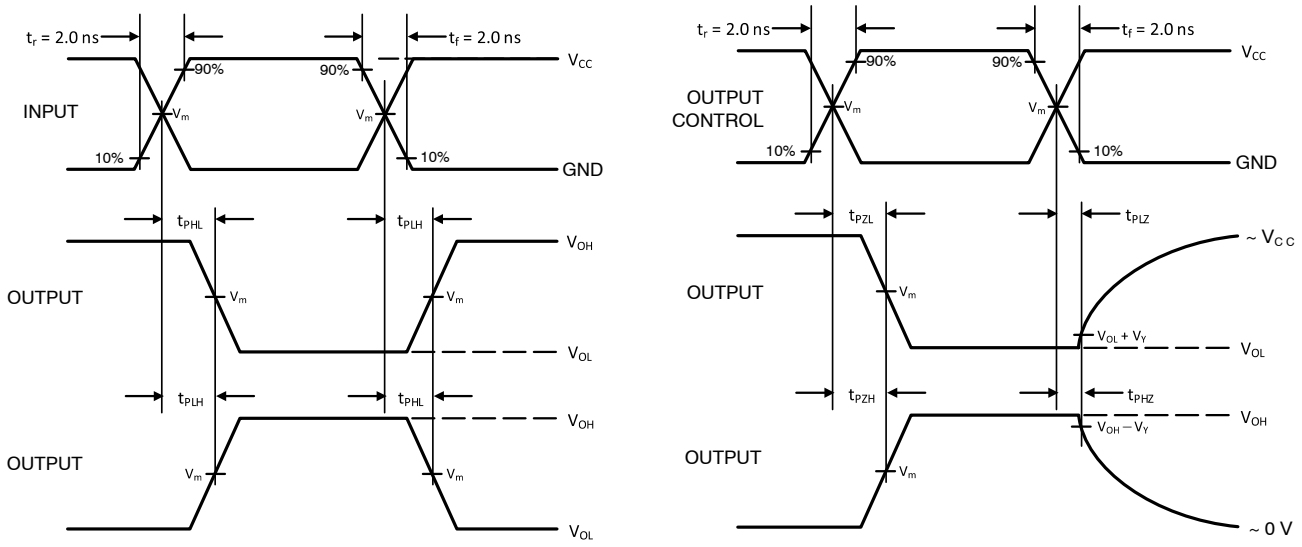
6. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	2 x VCC
t_{PHZ} / t_{PZH}	GND

C_L includes load and jig capacitance
Pulse generator Z_O = 50 Ω
Input f = 10 MHz; t_W = 500 ns

Figure 6. AC Test Circuit



V_{CC}, V	C_L, pF	R_L, Ω	V_m, V	V_Y, V
1.65 V to 1.95 V	15	500	$V_{CC}/2$	0.1
2.3 V to 2.7 V	30	500	$V_{CC}/2$	0.15
3.0 V to 3.6 V	50	500	$V_{CC}/2$	0.3

Figure 7. AC Waveforms

ORDERING INFORMATION

Device	Marking	Pin 1 Quadrant	Package	Shipping†
T30LMSW3B3257DR2G	TBD	1	SOIC-16	2500 / Tape & Reel
T30LMSW3B3257DTR2G	TBD	1	TSSOP-16	2500 / Tape & Reel
T30LMSW3B3257DSR2G	TBD	1	SSOP-16	TBD / Tape & Reel
T30LMSW3B3257MU2TAG	TBD	1	UQFN-16 (1.8 x 2.6)	3000 / Tape & Reel
T30LMSW3B3253DR2G	TBD	1	SOIC-16	2500 / Tape & Reel
T30LMSW3B3253DTR2G	TBD	1	TSSOP-16	2500 / Tape & Reel
T30LMSW3B3253DSR2G	TBD	1	SSOP-16	TBD / Tape & Reel
T30LMSW3B3125DR2G	TBD	1	SOIC-14	2500 / Tape & Reel
T30LMSW3B3125DTR2G	TBD	1	TSSOP-14	2500 / Tape & Reel
T30LMSW3B3125DSR2G	TBD	1	SSOP-14	TBD / Tape & Reel
T30LMSW3B3126DR2G	TBD	1	SOIC-14	2500 / Tape & Reel
T30LMSW3B3126DTR2G	TBD	1	TSSOP-14	2500 / Tape & Reel
T30LMSW3B3126DSR2G	TBD	1	SSOP-14	TBD / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pin 1 Orientation in Tape and Reel

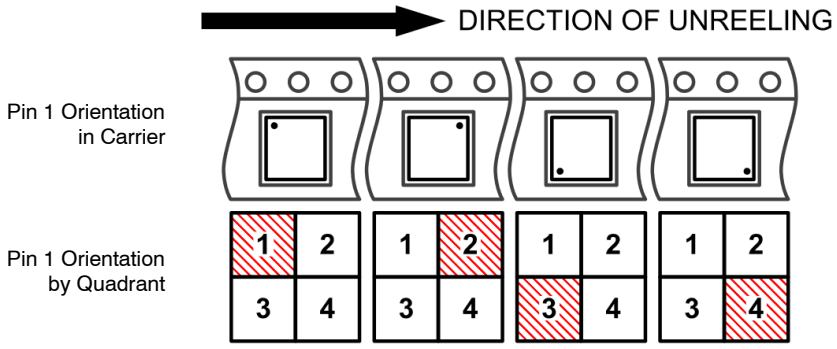
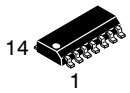


Figure 8.

PACKAGE DIMENSIONS



SCALE 1:1

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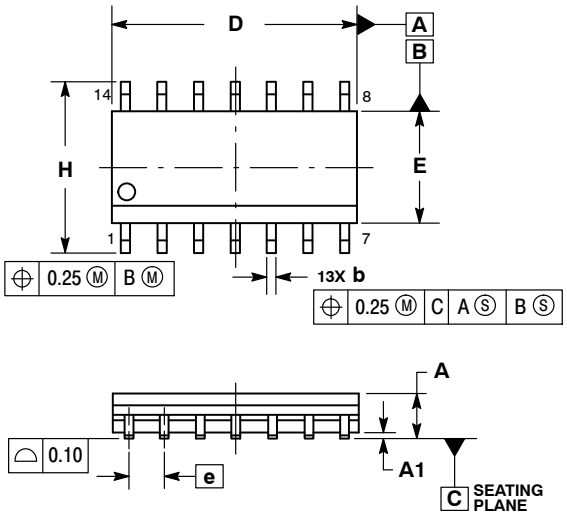
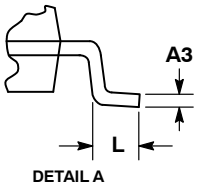
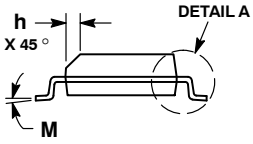
ISSUE L

DATE 03 FEB 2016



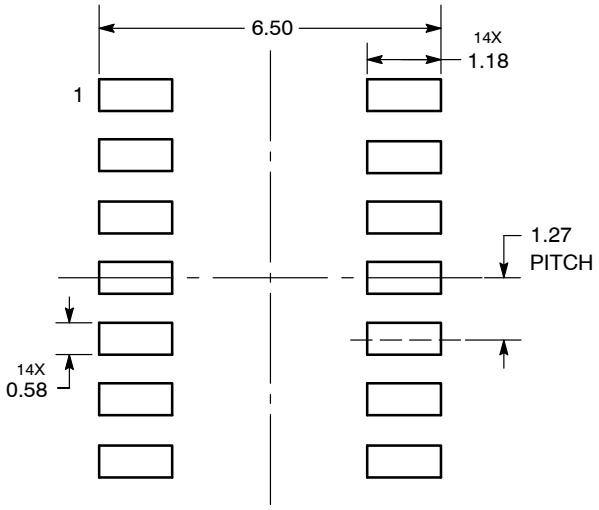




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

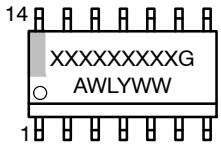
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

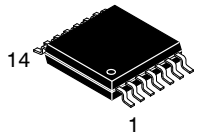
GENERIC MARKING DIAGRAM*



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

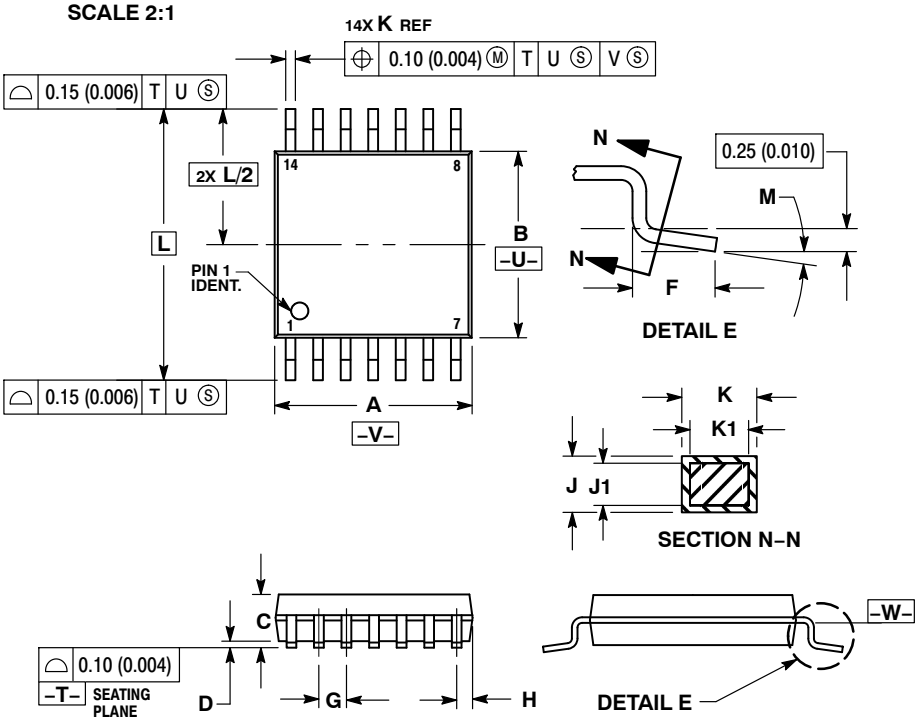
PACKAGE DIMENSIONS



SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

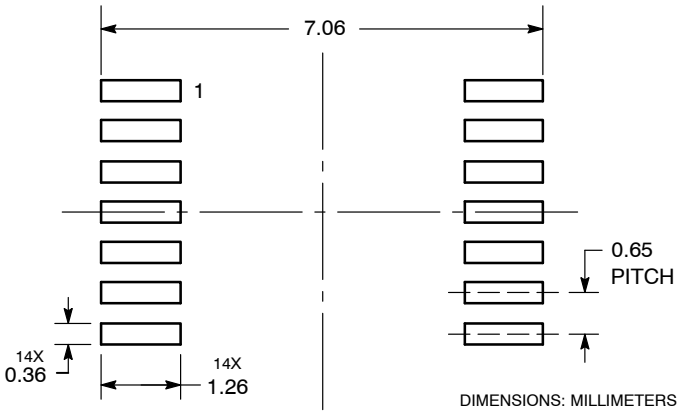
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

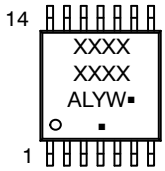
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

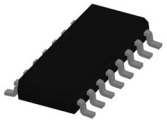


A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

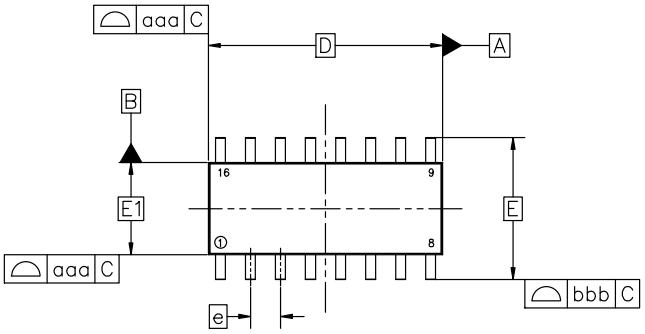
PACKAGE DIMENSIONS



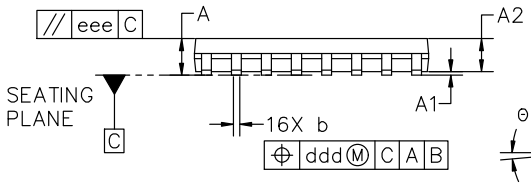
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

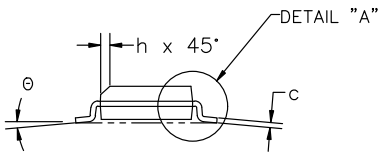
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



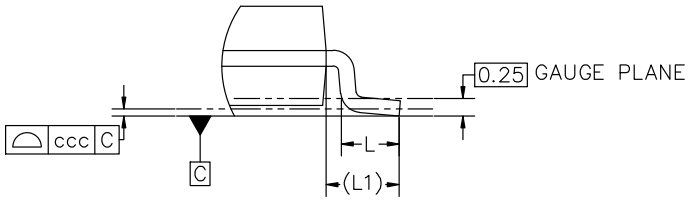
TOP VIEW



SIDE VIEW

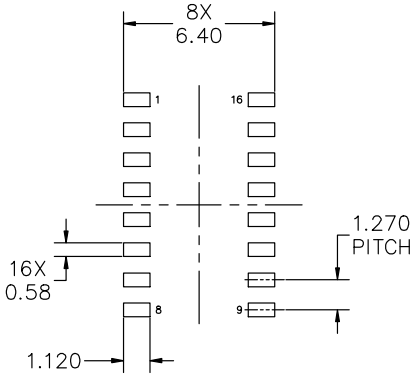


END VIEW



DETAIL "A"
Scale 3:1

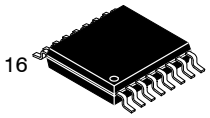
MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

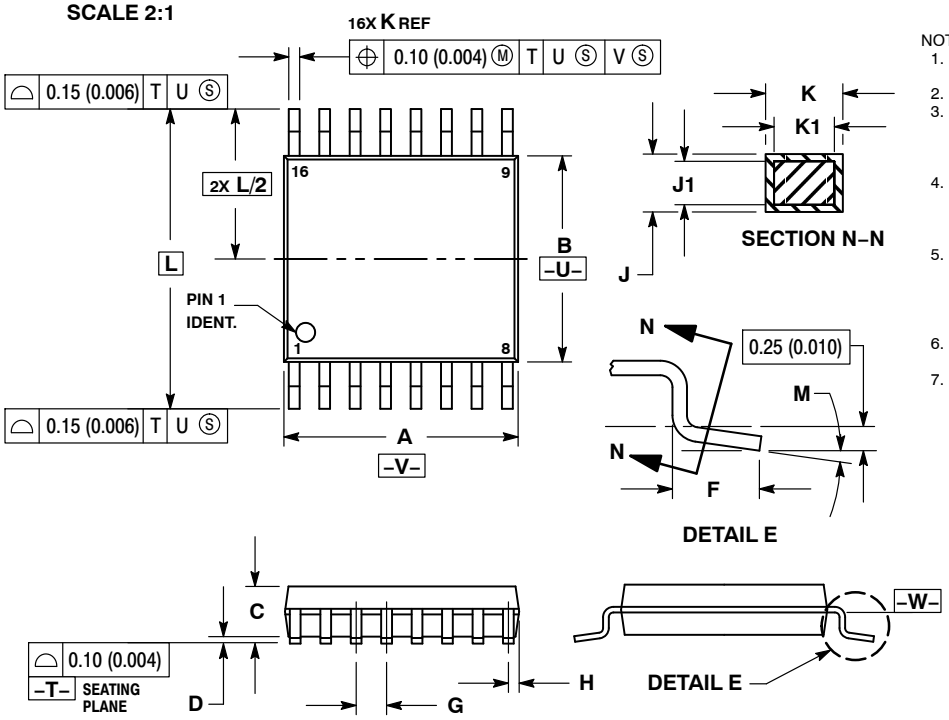
PACKAGE DIMENSIONS



SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

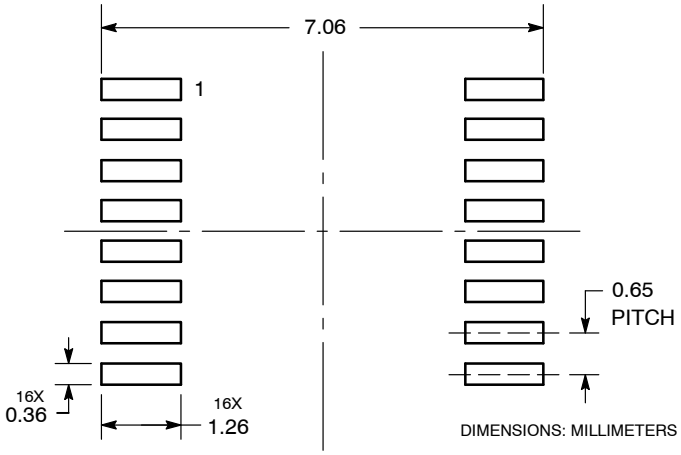
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

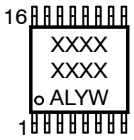
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



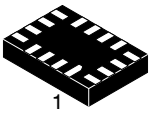
XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

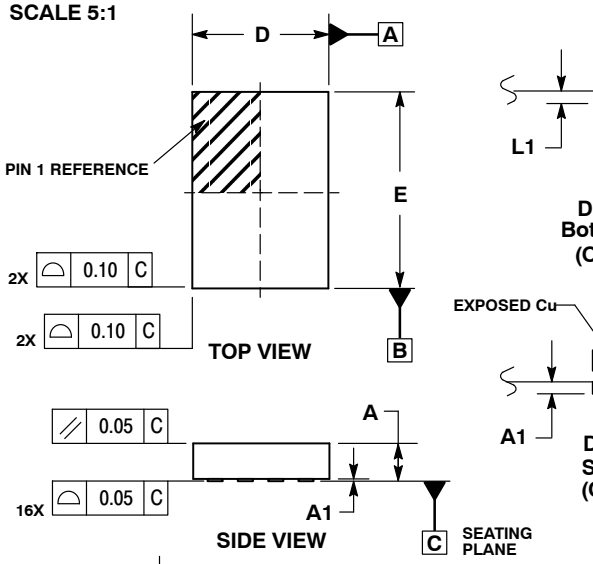
PACKAGE DIMENSIONS

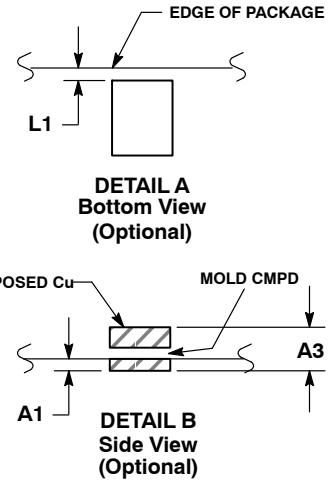
UQFN16 1.8x2.6, 0.4P
CASE 488AU
ISSUE A

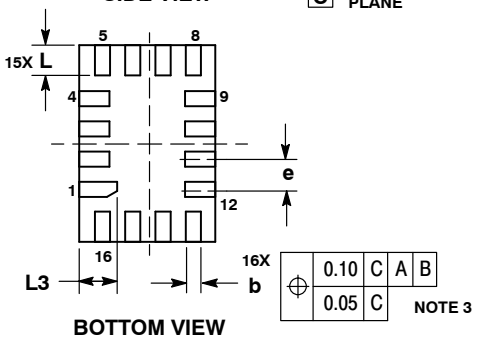
DATE 01 AUG 2007



SCALE 5:1



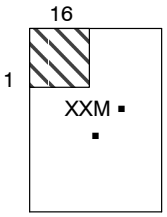




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.80 BSC	
E	2.60 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L3	0.40	0.60

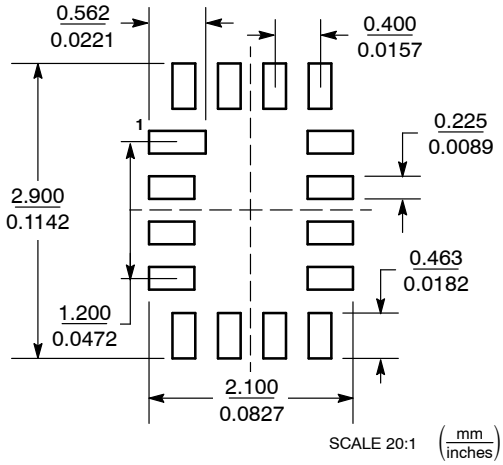
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code/Assembly Location
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

MOUNTING FOOTPRINT



SCALE 20:1 (mm / inches)

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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