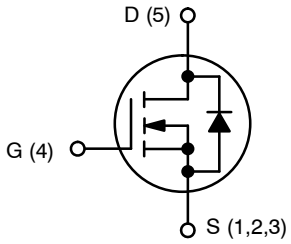
MOSFET – Power, Single, N-Channel, STD Gate, SO8FL

80 V, 6.2 mΩ, 73 A

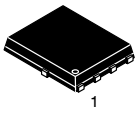
Product Preview

NTMFS6D2N08X

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	6.2 mΩ @ 10 V	73 A



N−CHANNEL MOSFET



DFN5
(SO−8FL)
CASE 488AA
STYLE 1

Features

- Low QRR, Soft Recovery Body Diode
- Low RDS(on) to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DCDC and ACDC
- Primary Switch in Isolated DCDC Converter
- Motor Drives

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	80	V
Gate−to−Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	73	A
	T_C = 100°C		52	
Power Dissipation	T_C = 25°C	P_D	68	W
Pulsed Drain Current	T_C = 25°C, t_p = 100 μs	I_{DM}	265	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Continuous Source−Drain Current (Body Diode)		I_S	115	A
Single Pulse Avalanche Energy (I_{PK} = 28 A)		E_{AS}	39	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 seconds)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal and electromechanical application board design.
3. EAS of 39 mJ is based on started T_J = 25°C, I_{AS} = 28 A, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested.

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

MARKING DIAGRAM

6D2N08 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS6D2N08XT1G	DFN5 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	39	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	80	–	–	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25°C	–	32	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25°C	–	–	1.0	μA
		V_{DS} = 80 V, T_J = 125°C	–	–	250	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 15 A, T_J = 25°C	–	5.1	6.2	mΩ
		V_{GS} = 6 V, I_D = 7 A, T_J = 25°C	–	7.7	11.8	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 75 μA, T_J = 25°C	2.4	–	3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 75 μA	–	−7	–	mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 15 A	–	48	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	–	1346	–	pF
Output Capacitance	C_{OSS}		–	388	–	
Reverse Transfer Capacitance	C_{RSS}		–	5.9	–	
Output Charge	Q_{OSS}			28		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{DD} = 40 V, I_D = 15 A, V_{GS} = 10 V	–	19	–	
Threshold Gate Charge	$Q_{G(TH)}$			4.1		
Gate−to−Source Charge	Q_{GS}		–	6.3	–	
Gate−to−Drain Charge	Q_{GD}		–	3.0	–	
Gate Plateau Voltage	V_{GP}			4.7		V
Gate Resistance	R_G	f = 1 MHz	–	1.6	–	Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 40 V, I_D = 15 A, R_G = 2.5 Ω	–	9.9	–	ns
Rise Time	t_r		–	19	–	
Turn−Off Delay Time	$t_{d(OFF)}$		–	15	–	
Fall Time	t_f		–	24	–	
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	I_S = 15 A, V_{GS} = 0 V, T_J = 25°C	–	0.82	1.2	V
		I_S = 15 A, V_{GS} = 0 V, T_J = 125°C	–	0.66	–	
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 15 A, dI/dt = 1000 A/μs, V_{DD} = 40 V, T_J = 25°C	–	18	–	ns
Charge Time	t_a		–	8.7	–	
Discharge Time	t_b		–	8.8	–	
Reverse Recovery Charge	Q_{RR}		–	83	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

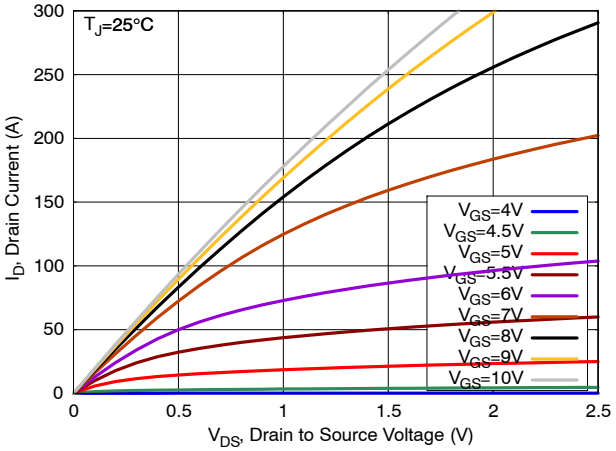


Figure 1. On−Region Characteristics

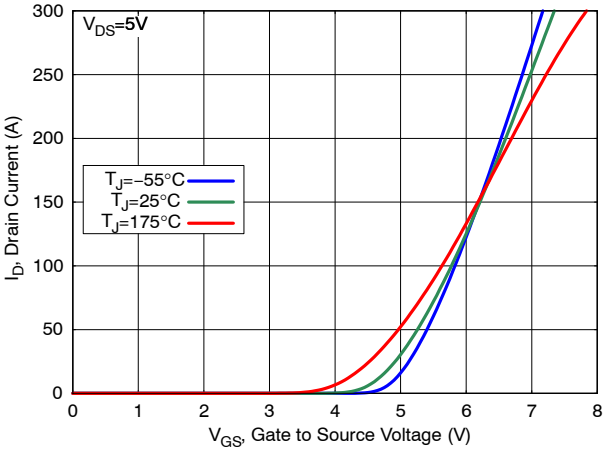


Figure 2. Transfer Characteristics

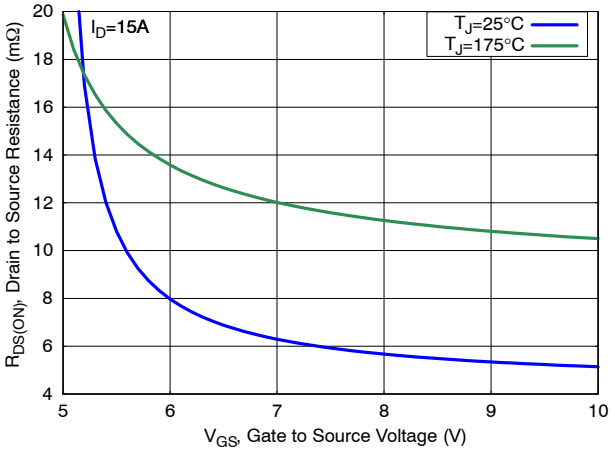


Figure 3. On−Resistance vs. Gate Voltage

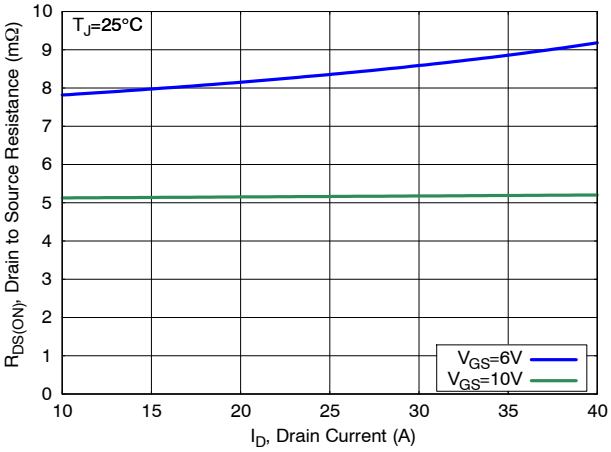


Figure 4. On−Resistance vs. Drain Current

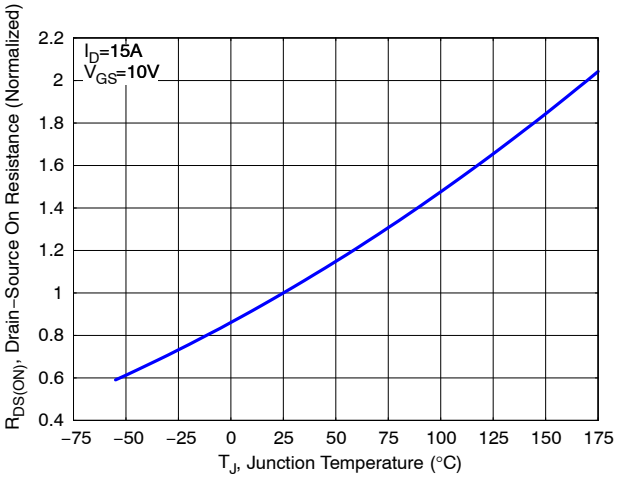


Figure 5. Normalized ON Resistance vs. Junction Temperature

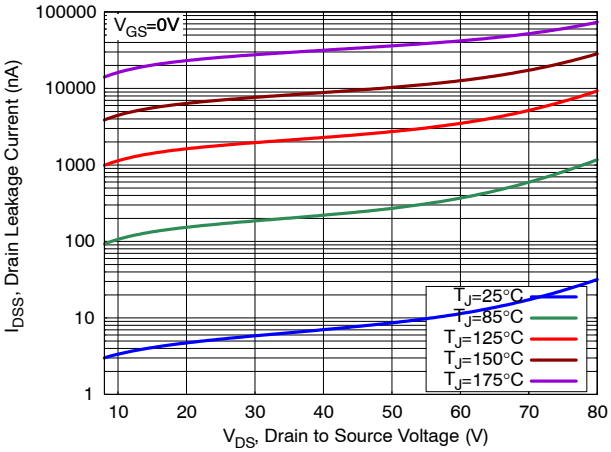


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

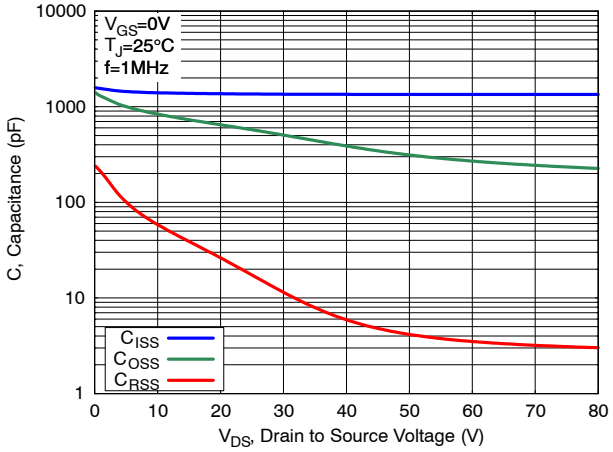


Figure 7. Capacitance Characteristics

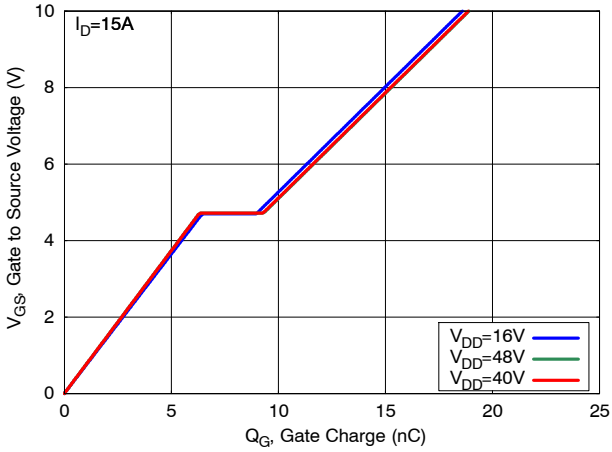


Figure 8. Gate Charge Characteristics

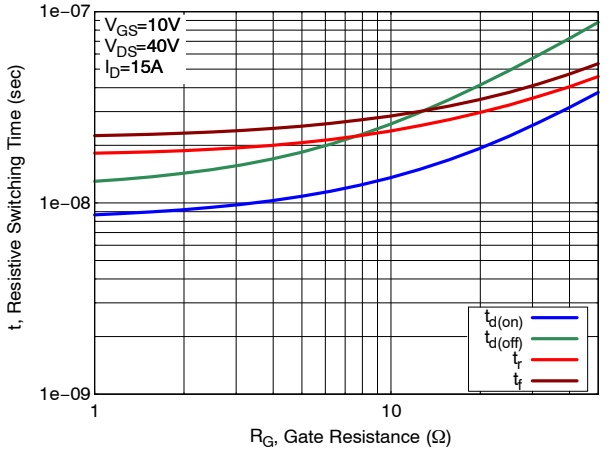


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

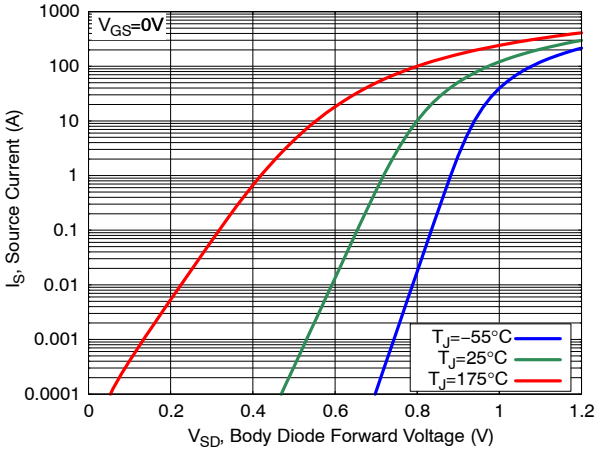


Figure 10. Diode Forward Characteristics

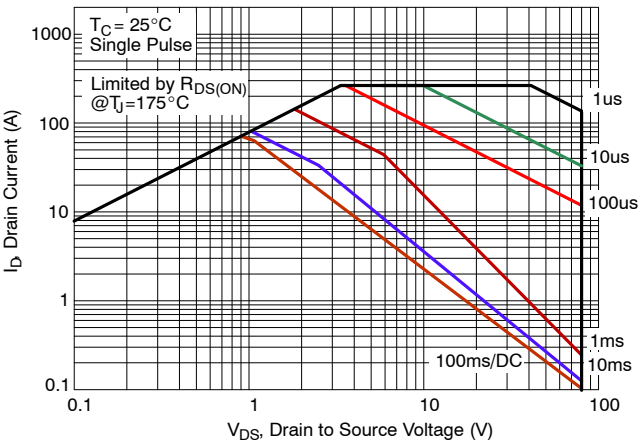


Figure 11. Safe Operating Area (SOA)

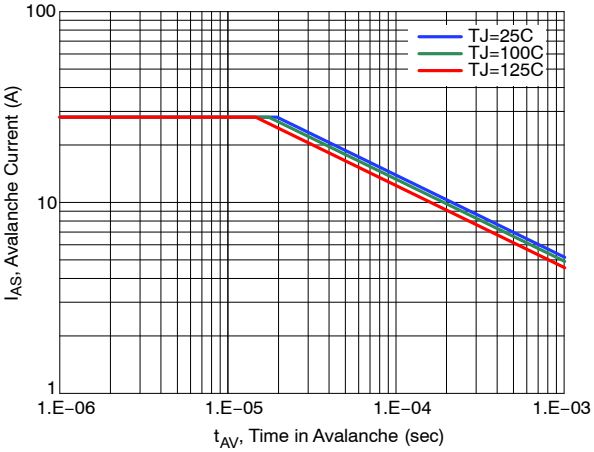


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

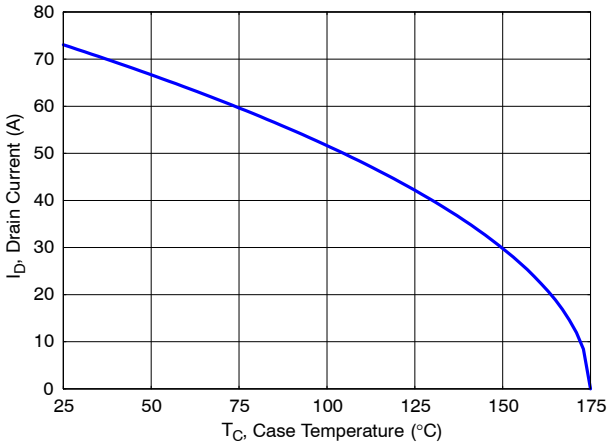


Figure 13. Maximum Current vs. Case Temperature

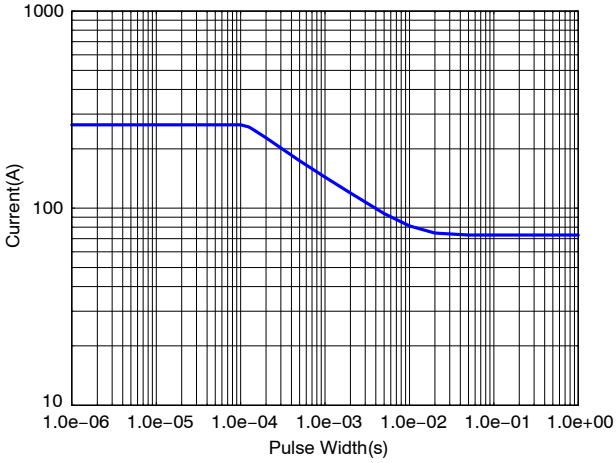


Figure 14. IDM vs. Pulse Width

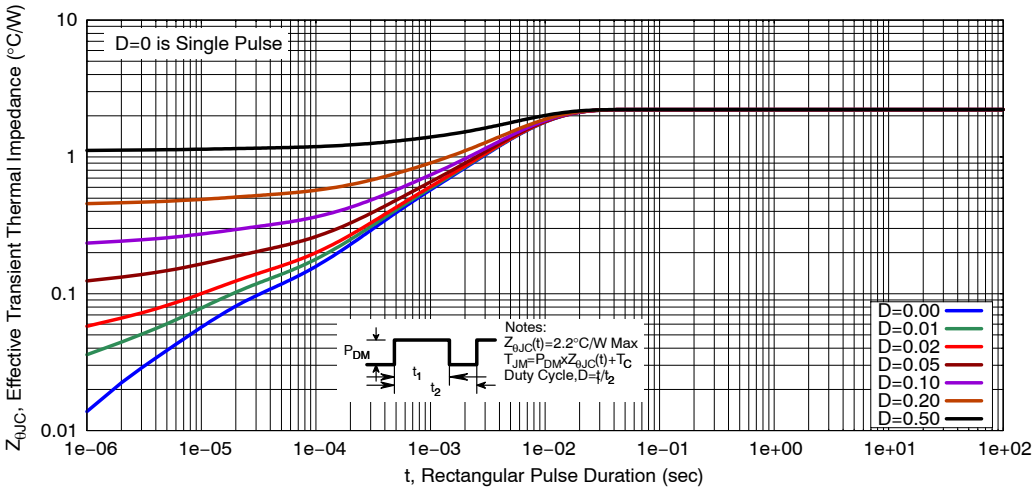
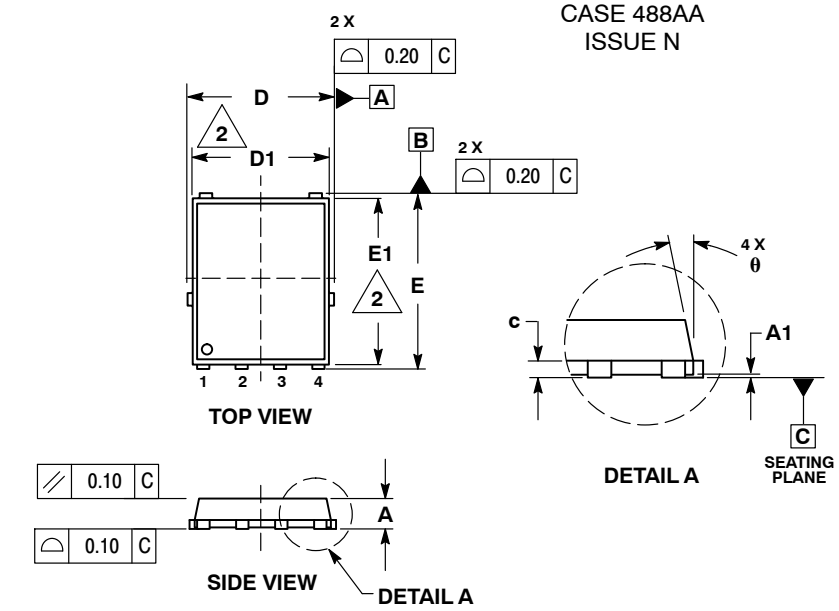
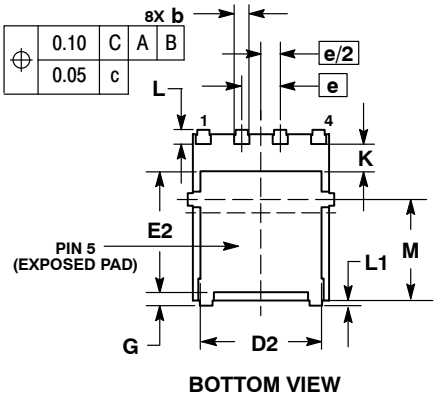


Figure 15. Transient Thermal Response

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N



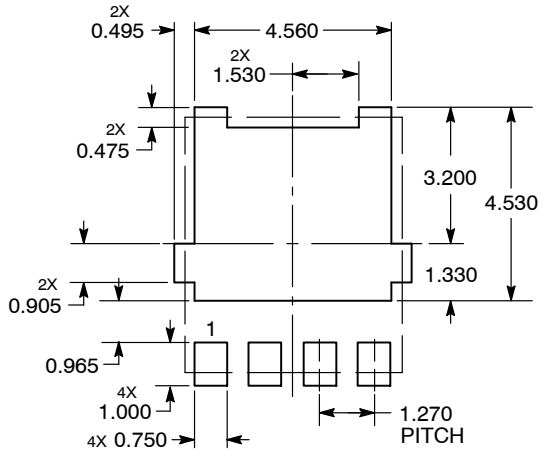


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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