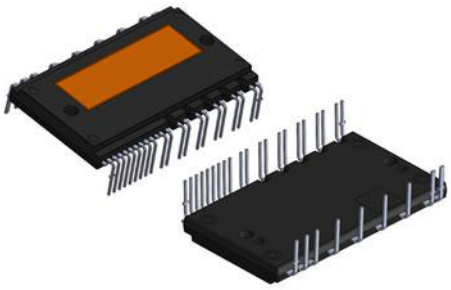
Intelligent Power Module (IPM)

Inverter, 1200 V, 50 A

NFAM3812SCBUT



CASE MODGC
DIP39, 54.5x31.0 EP−2

General Description

The NFAM3812SCBUT is a fully−integrated inverter power module consisting of an independent High side gate driver, LVIC, six SiC MOSFET's and a temperature sensor (VTS or Thermistor), suitable for driving permanent magnet synchronous (PMSM) motors, brushless DC (BLDC) motors and AC asynchronous motors. The MOSFET's are configured in a three−phase bridge with separate source connections for the lower legs for maximum flexibility in the choice of control algorithm.

The power stage has undervoltage lockout protection (UVP). Internal bootstrap diodes/resistors are provided for high side control.

Features

- 1200 V 50 A 3−Phase MOSFET Inverter, Including Control ICs for Gate Drive and Protections
- Active Logic Interface
- Built−in Under−voltage Protection (UVP)
- Built−in Bootstrap Diodes/Resistors
- Separate Low−side MOSFET Source Connections for Individual Current Sensing of Each Phase
- Temperature Sensor (VTS Output by LVIC or Thermistor)
- UL Certification: E209204
- This is a Pb−Free Device

Typical Application

- Industrial Drives
- Industrial Pumps
- Industrial Fans
- Industrial Automation

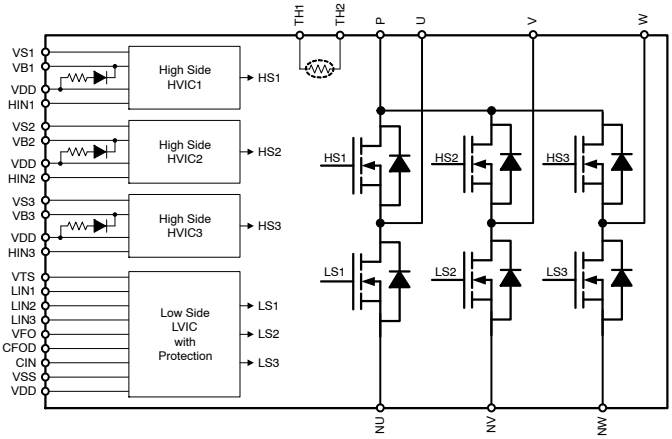
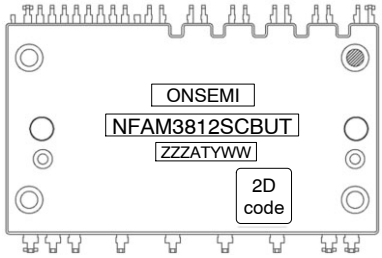


Figure 1. Pin Configuration − Top View

MARKING DIAGRAM



NFAM3812SCBUT = Specific Device Code
ZZZ = Assembly Lot Code
A = Assembly Location
T = Test Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
NFAM3812SCBUT	DIP39, 31.0 x 54.5	90 / BOX

PIN CONFIGURATION

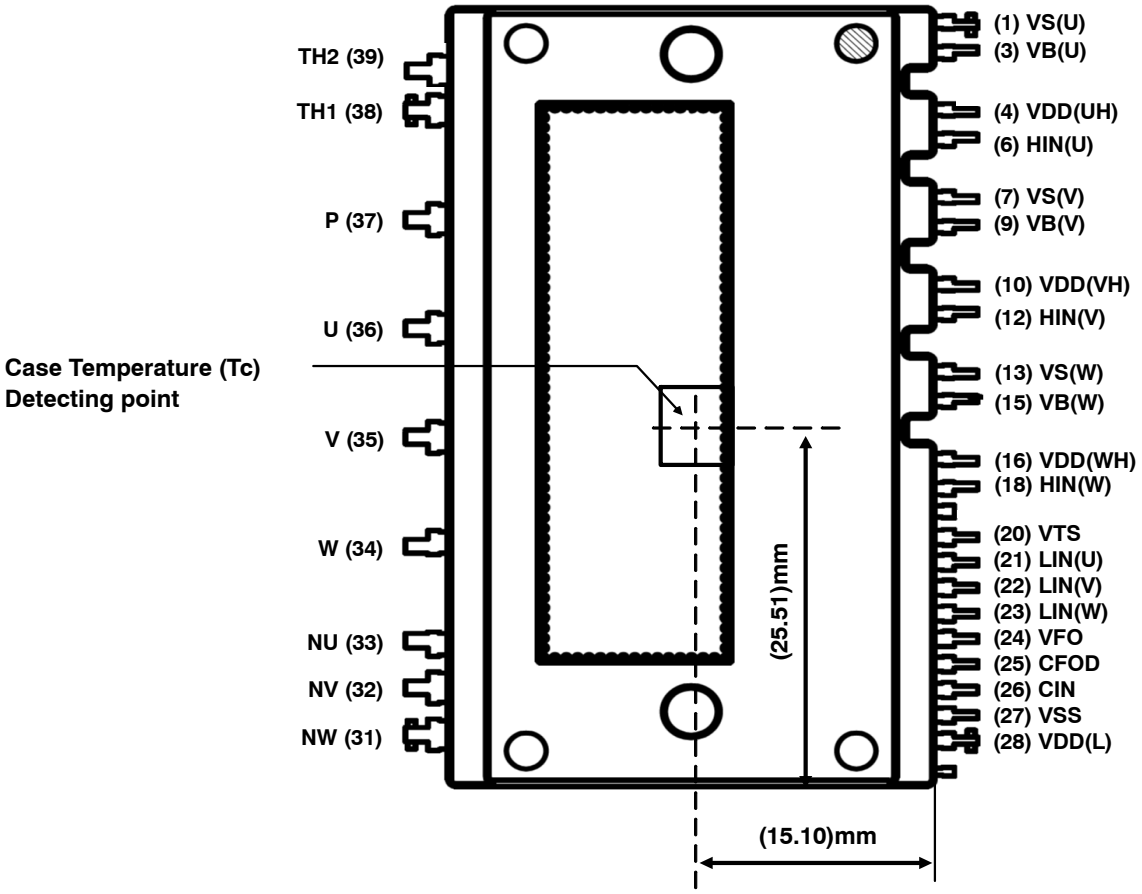


Figure 2. Pin Configuration – Top View

PIN DESCRIPTION

Pin	Name	Description
1	VS(U)	High−Side Bias Voltage Ground for U−Phase MOSFET Driving
(2)	−	Dummy
3	VB(U)	High−Side floating supply voltage for U−Phase MOSFET Driving
4	VDD(UH)	High−Side control power supply for U−Phase IC
(5)	−	Dummy
6	HIN(U)	Signal Input for High−Side U−Phase
7	VS(V)	High−Side Bias Voltage Ground for V−Phase MOSFET Driving
(8)	−	Dummy
9	VB(V)	High−Side floating supply voltage for V−Phase MOSFET Driving
10	VDD(VH)	High−Side control power supply for V−Phase IC
(11)	−	Dummy
12	HIN(V)	Signal Input for High−Side V−Phase
13	VS(W)	High−Side Bias Voltage Ground for W−Phase MOSFET Driving
(14)	−	Dummy
15	VB(W)	High−Side floating supply voltage for W−Phase MOSFET Driving
16	VDD(WH)	High−Side control power supply for W−Phase IC
(17)	−	Dummy
18	HIN(W)	Signal Input for High−Side W−Phase
(19)	−	Dummy
20	VTS	Output for LVIC Temperature Sensing Voltage
21	LIN(U)	Signal Input for Low−Side U−Phase
22	LIN(V)	Signal Input for Low−Side V−Phase
23	LIN(W)	Signal Input for Low−Side W−Phase
24	VFO	Fault Output
25	CFOD	Capacitor for Fault Output Duration Selection
26	CIN	Input for Current Protection
27	VSS	Low−Side Common Supply Ground
28	VDD(L)	Low−Side Bias Voltage for IC and MOSFETs Driving
(29)	−	Dummy
(30)	−	Dummy
31	NW	Negative DC−Link Input for W−Phase
32	NV	Negative DC−Link Input for V−Phase
33	NU	Negative DC−Link Input for U−Phase
34	W	Output for W−Phase
35	V	Output for V−Phase
36	U	Output for U−Phase
37	P	Positive DC−Link Input
38	TH1	Thermistor connection (T) / No connection
39	TH2	Thermistor connection *optional for T

NOTE: Pins of ( ) are the dummy for internal connection. These pins should be no connection.

INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS

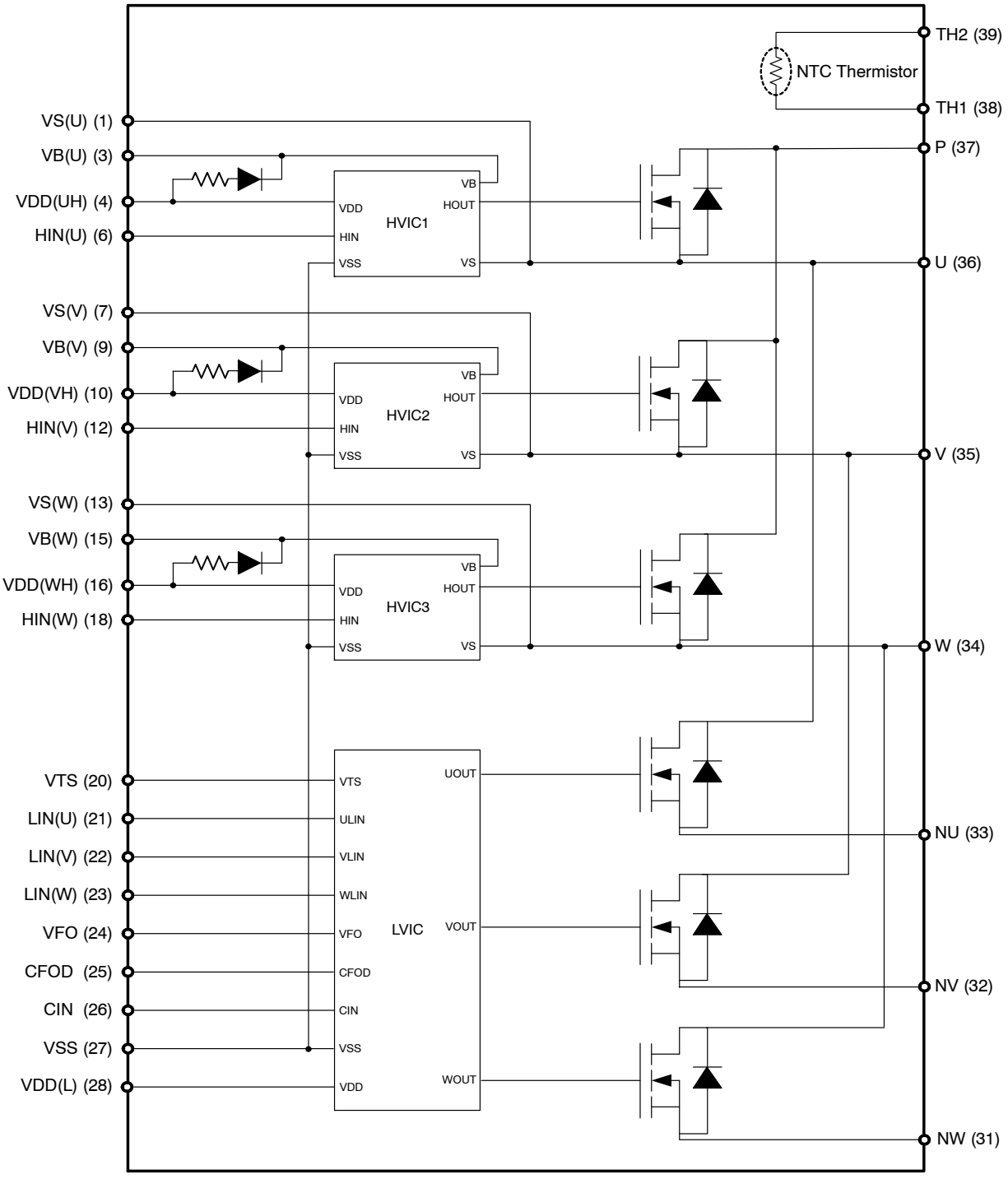


Figure 3. Internal Block Diagram

ABSOLUTE MAXIMUM RATINGS (VDD = 18 V and Tj = 25°C, Unless Otherwise Specified)

Symbol	Parameter	Test Condition	Max	Unit
INVERTER PART				
VPN	Supply Voltage	Applied between P – NU, NV, NW	900	V
VPN (surge)	Supply Voltage (Surge)	Applied between P – NU, NV, NW (Note 1)	1000	V
VDS	Drain–Source Voltage	P to U, V, W; U to NU, V to NV, W to NW	1200	V
ID	Output Current	P, NU, NV, NW, U, V, W terminal current	±50	A
IDP	Output Peak Current	P, NU, NV, NW, U, V, W terminal current pulse width 1 ms	±100	A
Pd	Power Dissipation	Tc = 25°C per One Chip (Note 2)	157	W
Tj	Operating Junction Temperature		–40 ~ 175	°C
CONTROL PART				
VDD	Control Supply Voltage	Applied between VDD(H), VDD(L) – VSS	20	V
VBS	High–Side Control Bias Voltage	Applied between VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)	20	V
VIN	Input Signal Voltage	Applied between HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) – VSS	–0.3 ~ VDD + 0.3	V
VFO	Fault Output Supply Voltage	Applied between VFO – VSS	–0.3 ~ VDD + 0.3	V
IFO	Fault Output Current	Sink Current at VFO pin	2	mA
VCIN	Current Sensing Input Voltage	Applied between CIN – VSS	–0.3 ~ VDD + 0.3	V
TOTAL SYSTEM				
VPN(prot)	Self–Protection Supply Voltage Limit (Short Circuit Protection Capability)	VDD = VBS = 13.5 V to 18.0 V, Tj = 150°C, Non–repetitive, less than 2 μs	800	V
Tc	Case Operation Temperature	See Figure 2	–40 ~ 150	°C
Tstg	Storage Temperature		–40 ~ 150	°C
Viso	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate	2500	V_{rms}

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminal.
2. Calculation value considered to design factor.

THERMAL RESISTANCE

Symbol	Rating	Conditions	Min	Typ	Max	Unit
θj–c(T)	Junction to Case Thermal Resistance (Note 3)	MOSFET per 1/6 module	–	–	0.95	°C/W

3. For the measurement point of case temperature (Tc), please refer to Figure 2.

ELECTRICAL CHARACTERISTICS (Tc = 25°C, VDD = 18 V, VBS = 18 V, unless otherwise noted) (Notes 8, 9)

Symbol		Description	Conditions		Min	Typ	Max	Unit
INVERTER PART								
IDSS		Drain − Source Leakage Current	VDS = 1200 V, Tj = 25°C		−	−	1	mA
			VDS = 1200 V, Tj = 150°C		−	−	10	mA
RDS(ON)		Drain to Source On Resistance	ID = 50 A, VDD = VBS = 18 V, Tj = 25°C		−	38	55	mΩ
			ID = 50 A, VDD = VBS = 18 V, Tj = 150°C		−	67	−	mΩ
VSD		Diode Forward Voltage	VDD = VBS = 18 V, ISD = 50 A, Tj = 25°C	HIN/LIN = OFF	−	4.55	5.25	V
				HIN/LIN = ON	−	1.53	2.35	V
			VDD = VBS = 18 V, HIN/LIN = ON, ISD = 50 A, Tj = 150°C	HIN/LIN = OFF	−	5.30	−	V
				HIN/LIN = ON	−	2.80	−	V
Switching times	ton	High Side Switching Times	VPN = 600 V, VDD = 18 V, ID = 50 A Tj = 25°C, Inductive Load Switching See Figure 4, 25, 26 (Note 4)		0.55	1.05	1.55	μs
	tc(on)				−	0.15	0.55	μs
	toff				−	1.05	1.45	μs
	tc(off)				−	0.08	0.15	μs
	trr				−	0.15	−	μs
Eon		Turn−on switching loss	ID = 50 A, VPN = 600 V, Tj = 25°C		−	1.95	−	mJ
Eoff		Turn−off switching loss				1.70	−	mJ
Eon		Turn−on switching loss	ID = 50 A, VPN = 600 V, Tj = 150°C		−	1.85	−	mJ
Eoff		Turn−off switching loss				2.00	−	mJ
Erec		Diode reverse recovery energy	ID = 50 A, VPN = 600 V, (di/dt set by internal driver)	Tj = 25°C	−	0.15	−	mJ
				Tj = 150°C	−	0.20	−	
CONTROL PART								
IQDDH		Quiescent VDD Supply Current	VDD(UH, VH, WH) = 18 V, HIN(U,V,W) = 0 V	VDD(UH) − VSS VDD(VH) − VSS VDD(WH) − VSS	−	−	0.3	mA
IQDDL			VDD(L) = 18 V, LIN(U, V, W) = 0 V	VDD(L) − VSS	−	−	2.5	mA
IPDDH		Operating VDD Supply Current	VDD(UH, VH, WH) = 18 V, fPWM = 60 kHz, duty = 50%, applied to one PWM Signal Input for High−Side	VDD(UH) − VSS VDD(VH) − VSS VDD(WH) − VSS	−	−	0.4	mA
IPDDL			VDD(L) = 18 V, fPWM = 60 kHz, duty = 50%, applied to one PWM Signal Input for Low−Side	VDD(L) − VSS	−	−	6.0	mA
IQBS		Quiescent VBS Supply Current	VBS(U, V, W) = 18 V, HIN(U, V, W) = 0 V	VB(U) − VS(U), VB(V) − VS(V), VB(W) − VS(W)	−	−	0.4	mA
IPBS		Operating VBS Supply Current	VDD(UH,VH,WH) = VBS(U, V, W) = 18 V, fPWM = 60 kHz, duty = 50%, applied to one PWM Signal Input for High−Side	VB(U) − VS(U), VB(V) − VS(V), VB(W) − VS(W)	−	−	4.0	mA
VIN(ON)		ON Threshold Voltage	HIN(U, V, W) − VSS, LIN(U, V, W) − VSS		−	−	2.6	V
VIN(OFF)		OFF Threshold Voltage			0.8	−	−	V
VIN hys		Input Voltage Threshold Hysteresis			−	−	2.6	V
IIN+		Input Current	VIN = 5 V		0.7	1	1.5	mA
VCIN(ref)		Over Current Trip Level	VDD = 18 V	CIN − VSS	0.46	0.48	0.50	V
UVDDD		Supply Circuit Under−Voltage Protection	VDD supply undervoltage negative going input threshold		10.3	−	12.5	V
UVDDR			VDD supply undervoltage positive going input threshold		10.8	−	13.0	V

ELECTRICAL CHARACTERISTICS (Tc = 25°C, VDD = 18 V, VBS = 18 V, unless otherwise noted) (Notes 8, 9)

Symbol	Description	Conditions	Min	Typ	Max	Unit
CONTROL PART						
UVBSD	Supply Circuit Under−Voltage Protection	VBS supply undervoltage negative going input threshold	10.0	–	12.0	V
UVBSR		VBS supply undervoltage positive going input threshold	10.5	–	12.5	V
VTS	Voltage Output for LVIC Temperature Sensing Unit	Pull down R = 5.1 kΩ, Temp. = 85°C	2.50	2.63	2.76	V
VFOH	Fault Output Voltage	VDD(L) = 0 V, CIN = 0 V, VFO Circuit: 10 kΩ to 5 V Pull−up	4.9	–	–	V
VFOL		VDD(L) = 0 V, CIN = 1 V, VFO Circuit: 10 kΩ to 5 V Pull−up	–	–	0.95	V
tFOD	Fault−Out Pulse Width	CFOD = 22 nF (Note 6)	1.6	2.2	–	ms
BOOTSTRAP PART						
VF BD	Bootstrap Diode Forward Current	If = 0.1 A (See Figure 7)	2.1	2.5	2.9	V
R BOOT	Built−in Limiting Resistance		12.5	15.5	18.5	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES: Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at Tj = Ta = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible. Values based on design and/or characterization.

4. ton and toff include the propagation delay of the internal drive IC. tc(on) and tc(off) are the switching times of MOSFET under the given gate−driving condition internally. For the detailed information, please see Figure 4.
5. TLVIC is the temperature of LVIC itself. VTS is only for sensing temperature of LVIC and cannot shutdown MOSFETs automatically. The relationship between VTS voltage output and LVIC temperature is described in Figure 5. It is recommended to add 5.1k Ω pull down resistor between VTS and VSS (Signal Ground) as described in Figure 6 for linear output characteristics at low temperature. To reduce noise, 10 nF cap is recommended as well. Refer to the application note for usage of VTS.
6. The fault−out pulse width tFOD depends on the capacitance value of CFOD according to the following approximate equation: tFOD = 0.1 x 10^6 x CFOD [s].

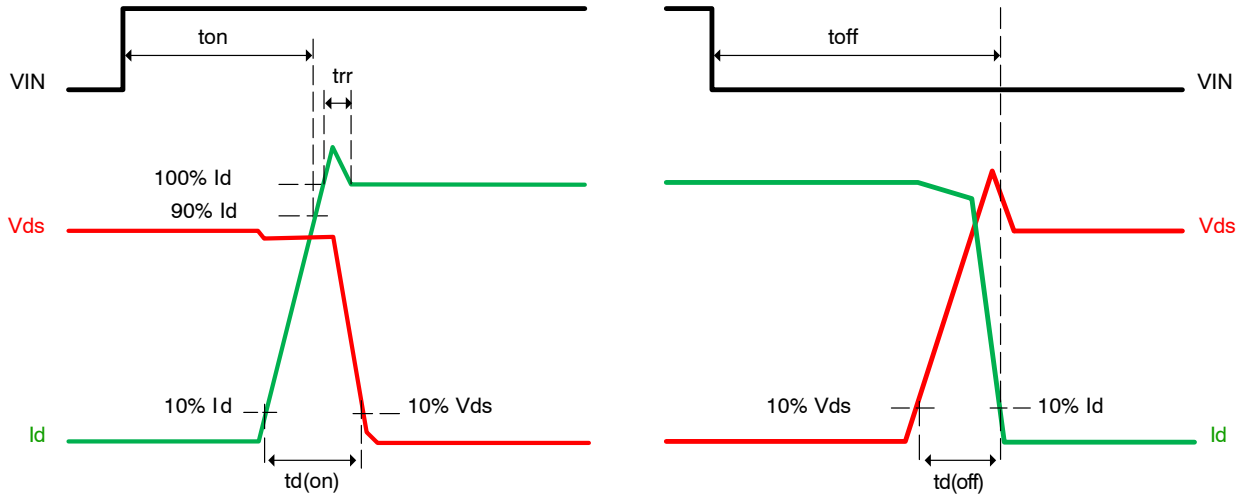


Figure 4. Switching Time Definitions

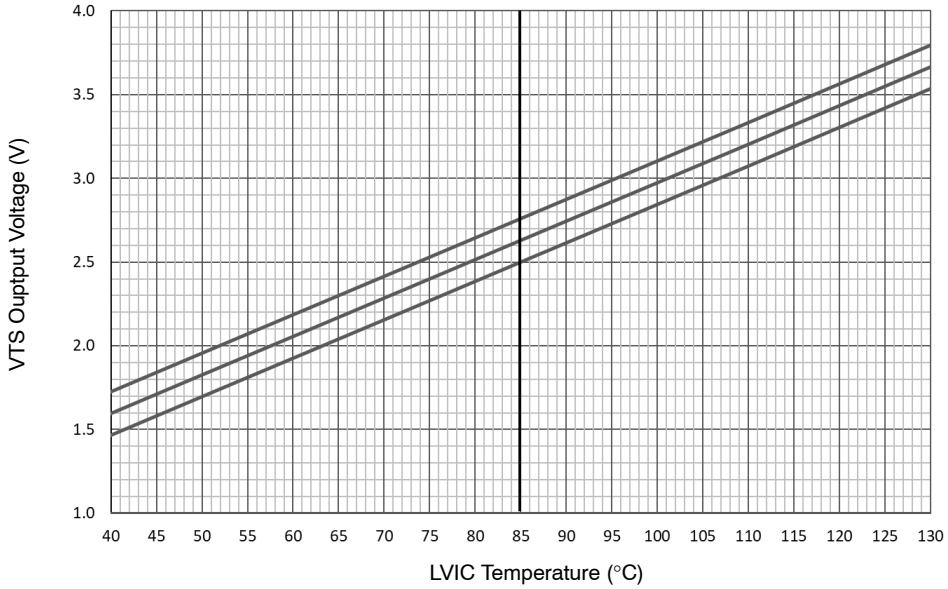


Figure 5. Temperature of LVIC versus VTS Characteristics

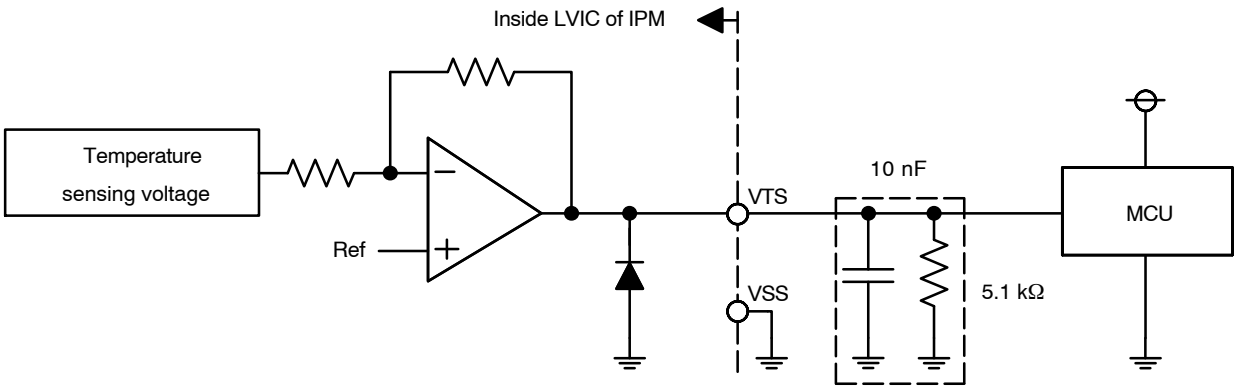


Figure 6. Internal Block Diagram and Interface Circuit of VTS

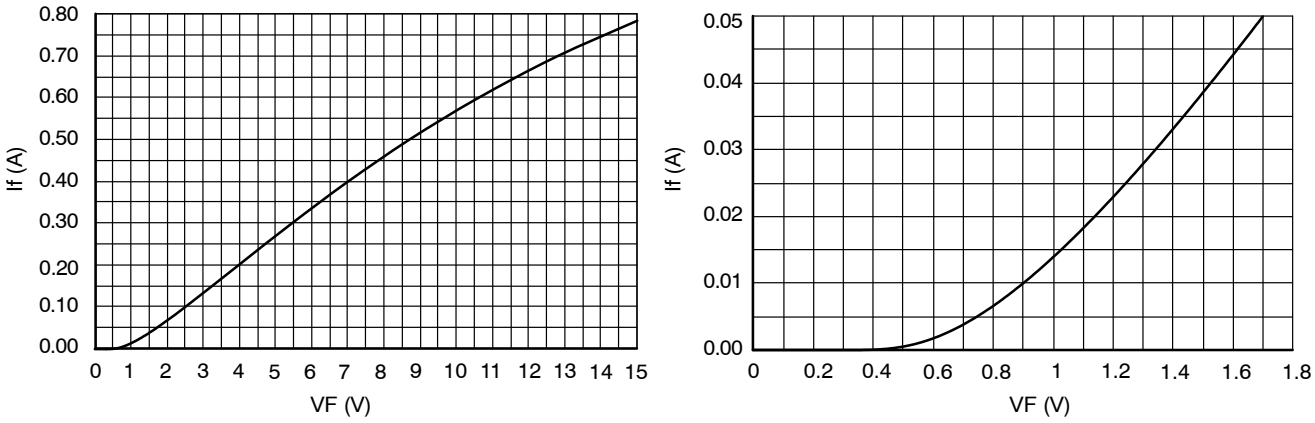


Figure 7. Characteristics of Bootstrap Diode/Resistor (Right Figure is Enlarged Figure)

THERMISTOR CHARACTERISTICS (Included only in NFAM3812SCBUT)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25°C	46.530	47	47.47	kΩ
Resistance	R_{125}	Tc = 100°C	1.344	1.406	1.471	kΩ
B−Constant (25−50°C)	−	B	4009.5	4050	4090.5	K
Temperature range	−	−	−40	−	+125	°C

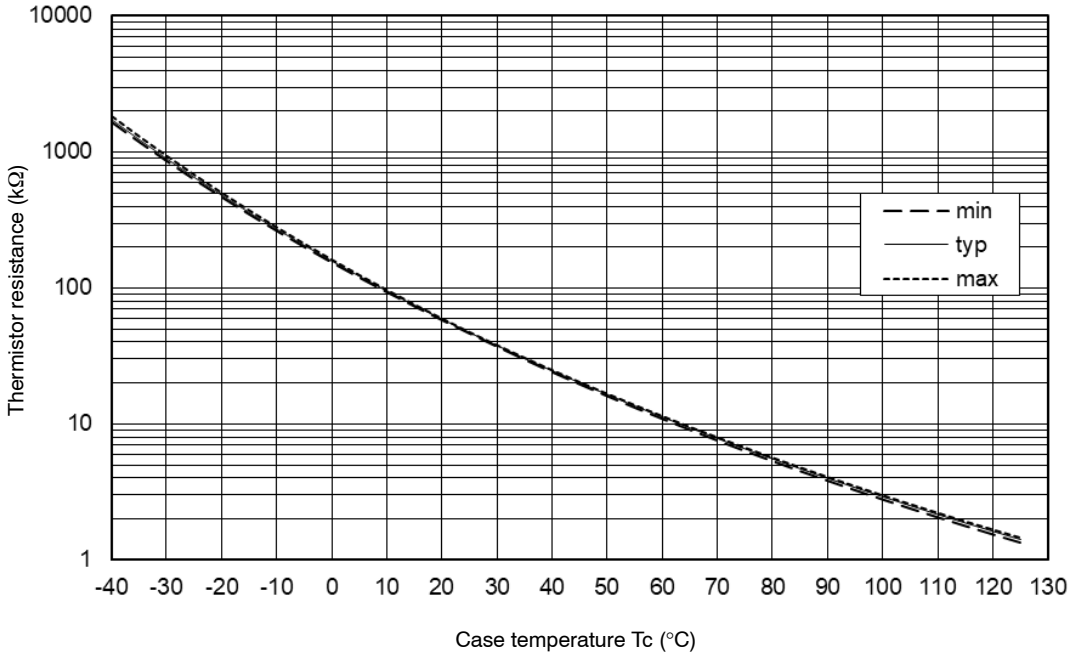


Figure 8. Thermistor Resistance versus Case Temperature

RECOMMENDED OPERATING CONDITIONS

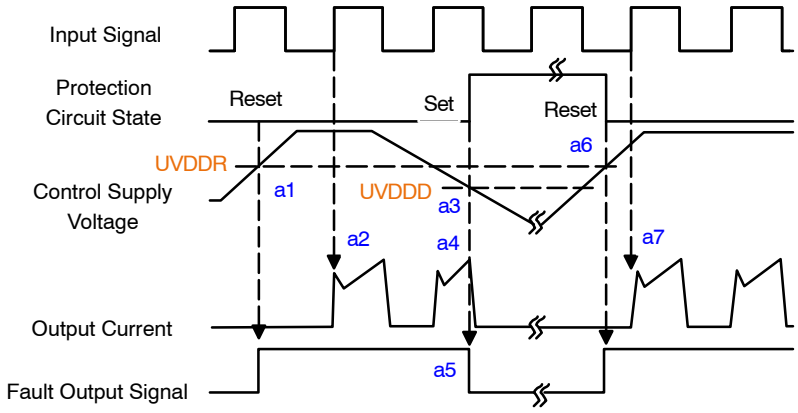
Symbol	Rating	Conditions		Min	Typ	Max	Unit
VPN	Supply Voltage	Applied between P – NU, NV, NW		–	600	800	V
VDD	Control Supply Voltage	Applied between VDD(H) – VSS, VDD(L) – VSS		13.0	18.0	19.0	V
VBS	High–Side Bias Voltages	Applied between VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)		13.5	18.0	19.5	V
dVDD / dt dVBS / dt	Supply Voltage Variation			–1	–	1	V / μs
DT	Dead Time	Turn–off to Turn–on (external)		0.80	–	–	μs
fPWM	PWM Input Signal	–40°C ≤ Tc ≤ 125°C, –40°C ≤ Tj ≤ 150°C		–	–	60	kHz
Io	Allowable r.m.s. Current	VPN = 600 V, VDD = VBS = 18 V, P.F. = 0.8, Tc ≤ 125°C, Tj ≤ 150°C, (Note 7)	fPWM = 5 kHz	–	–	27.0	A rms
			fPWM = 15 kHz	–	–	23.0	
			fPWM = 30 kHz	–	–	18.5	
PWIN(ON)	Minimum Input Pulse Width	VDD = VBS = 18 V, Wiring Inductance between NU,V,W and DC Link N < 10 nH (Note 8)		1.0	–	–	μs
PWIN(OFF)				1.0	–	–	
Package Mounting Torque		M3 Type Screw		0.6	0.7	0.9	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Flatness tolerance of the heatsink should be within –50 μm to +100 μm.

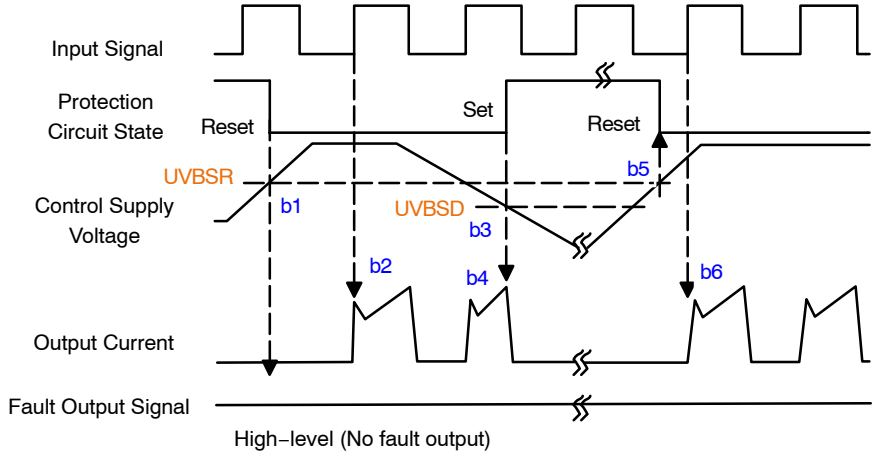
7. Allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition.
8. Product might not make response if input pulse width is less than the recommended value.

Time Charts of Protective Function



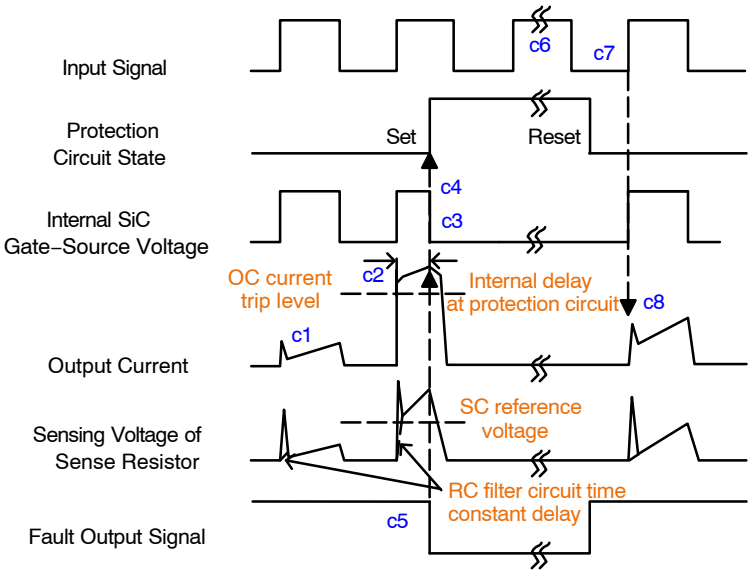
a1 : Control supply voltage rises: After the voltage rises UVDDR, the circuits start to operate when next input is applied.
a2 : Normal operation: MOSFET ON and carrying current.
a3 : Under voltage detection (UVDDD).
a4 : MOSFET OFF in spite of control input condition.
a5 : Fault output operation starts with a fixed pulse width.
a6 : Under voltage reset (UVDDR).
a7 : Normal operation: MOSFET ON and carrying current by triggering next signal from LOW to HIGH.

Figure 9. Under–Voltage Protection (Low–Side)



b1 : Control supply voltage rises: After the voltage reaches UVBSR, the circuits start to operate when next input is applied.
b2 : Normal operation: MOSFET ON and carrying current.
b3 : Under voltage detection (UVBSD).
b4 : MOSFET OFF in spite of control input condition, but there is no fault output signal.
b5 : Under voltage reset (UVBSR).
b6 : Normal operation: MOSFET ON and carrying current by triggering next signal from LOW to HIGH.

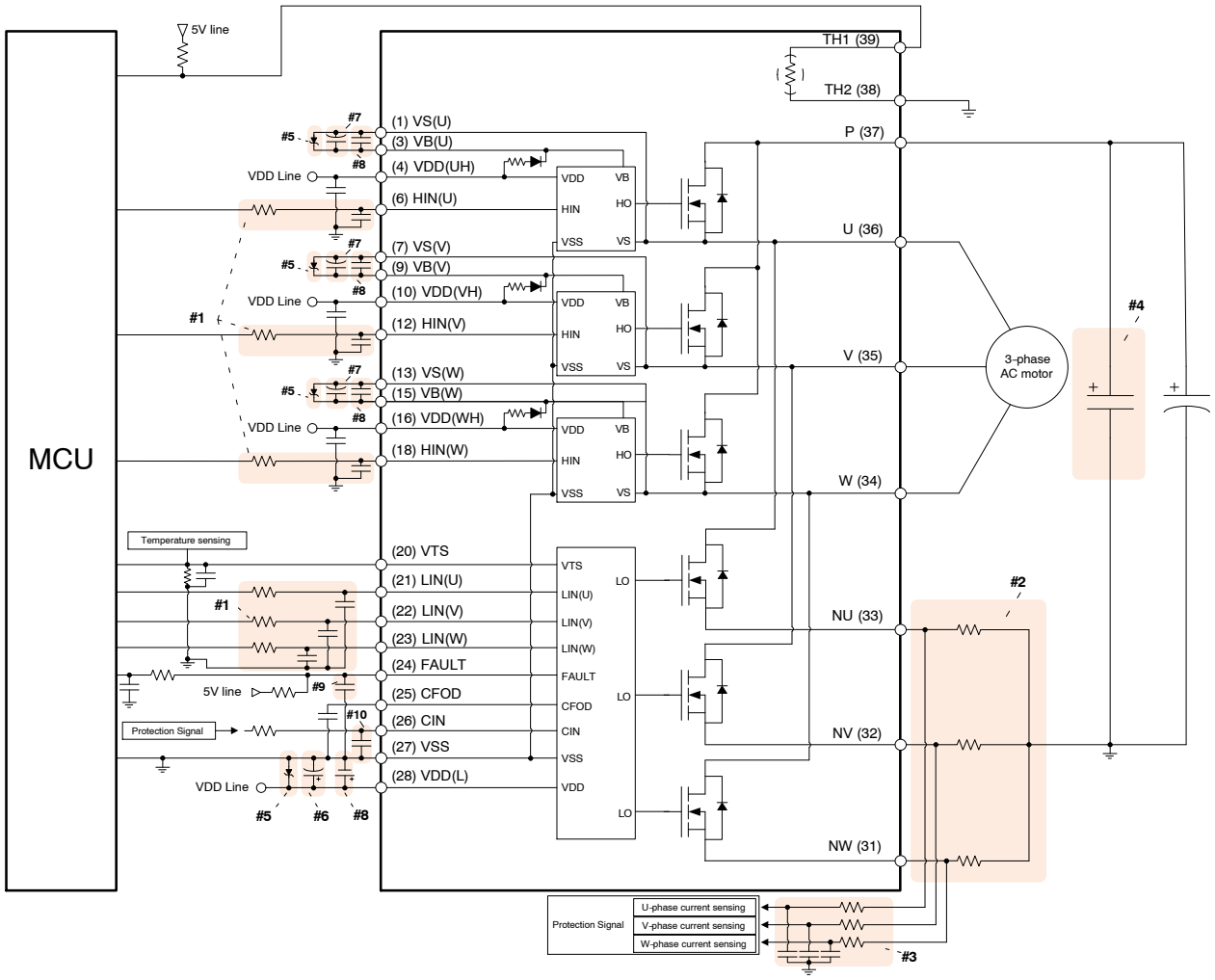
Figure 10. Under−Voltage Protection (High−Side)



(with the external sense resistance and RC filter connection)
c1 : Normal operation: MOSFET ON and carrying current.
c2 : Short circuit current detection (SC trigger).
c3 : All low−side MOSFET's gate are hard interrupted.
c4 : All low−side MOSFET's turn OFF.
c5 : Fault output operation starts with a fixed pulse width.
c6 : Input HIGH: MOSFET ON state, but during the active period of fault output the MOSFET doesn't turn ON.
c7 : Fault output operation finishes, but MOSFET doesn't turn on until triggering next signal from LOW to HIGH.
c8 : Normal operation: MOSFET ON and carrying current.

Figure 11. Short−Circuit Current Protection (Low−Side Operation only)

TYPICAL APPLICATION CIRCUIT



To avoid malfunction, the wiring of each input should be as short as possible (less than 2−3 cm). Each capacitor should be mounted as close to the pins of the product as possible. VFO output is open−drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes IFO up to 1 mA. Please refer to Figure 6.

NOTES:

9. Input signal is active−HIGH type. There is a 5 kΩ resistor inside the IC to pull−down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. RC time constant should be selected in the range 50 ~ 150 ns. (Recommended R = 100 Ω , C = 1 nF)
10. Each wiring pattern inductance should be minimized (Recommend less than 10 nH). Use the shunt resistor of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring should be connected to the terminal of the shunt resistor as close as possible.
11. In the short−circuit protection circuit, please select the RC time constant in the range 1.5 ~ 2 μs. Do enough evaluation on the real system because short−circuit protection time may vary wiring pattern layout and value of the RC time constant.
12. To prevent surge destruction, the wiring between the snubber capacitor and the P & GND pins should be as short as possible. The use of a high−frequency non−inductive capacitor of around 0.1 ~ 0.22 μF between the P & GND pins is recommended.
13. The Zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (Recommended Zener diode is 22 V / 1 W, which has the lower Zener impedance characteristic than about 15 Ω).
14. VDD electrolytic capacitor is recommended around 7 times larger than VBS electrolytic bootstrap capacitor.
15. Please choose the VBS electrolytic bootstrap capacitor with good temperature characteristic.
16. 0.1 ~ 0.2 μF R−category ceramic capacitors with good temperature and frequency characteristics is recommended.
17. Fault out pulse width can be adjusted by capacitor connected to the CFOD terminal.
18. To prevent protection function errors, CIN capacitor should be placed as close to CIN and VSS pins as possible.

Figure 12. Typical Application Circuit

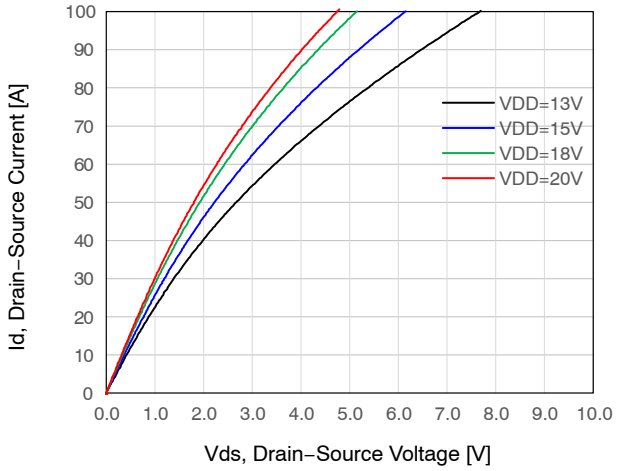


Figure 13. Typ. Drain–Source Saturation Voltage

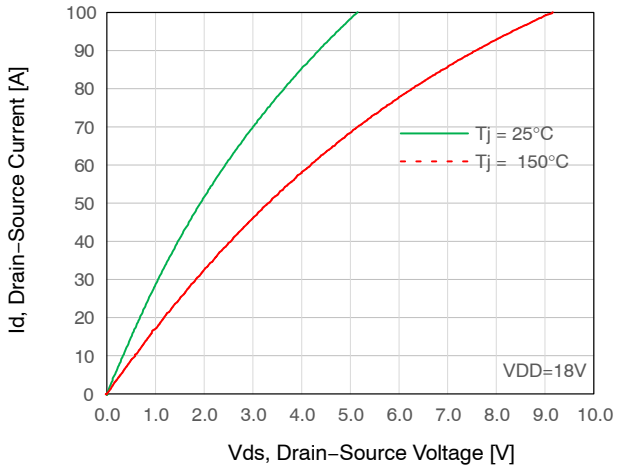


Figure 14. Drain–Source Saturation Voltage

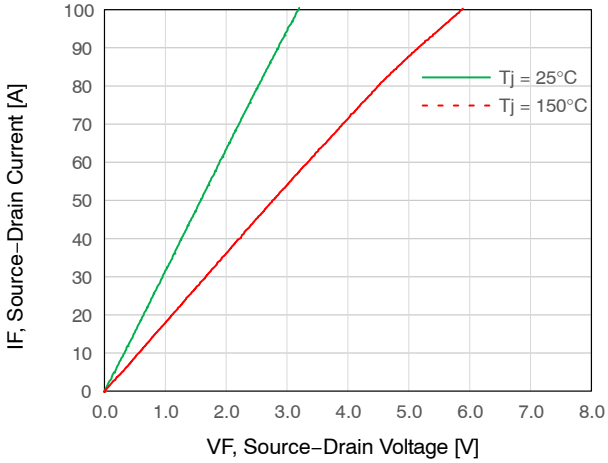


Figure 15. Typ. Source–Drain Forward Voltage

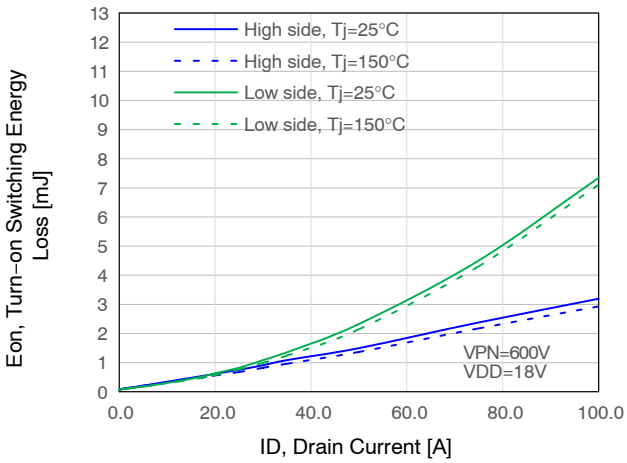


Figure 16. Typ. Turn–on Switching Energy Loss

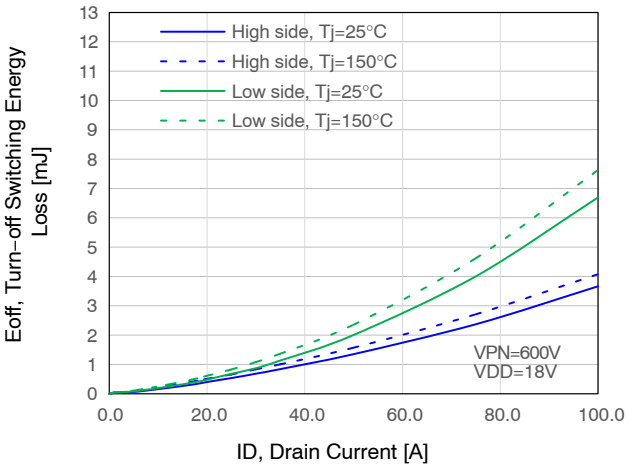


Figure 17. Typ. Turn–off Switching Energy Loss

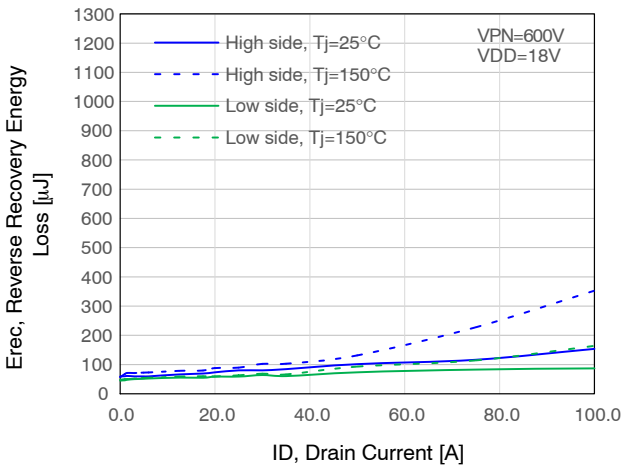


Figure 18. Typ. Reverse Recovery Energy Loss

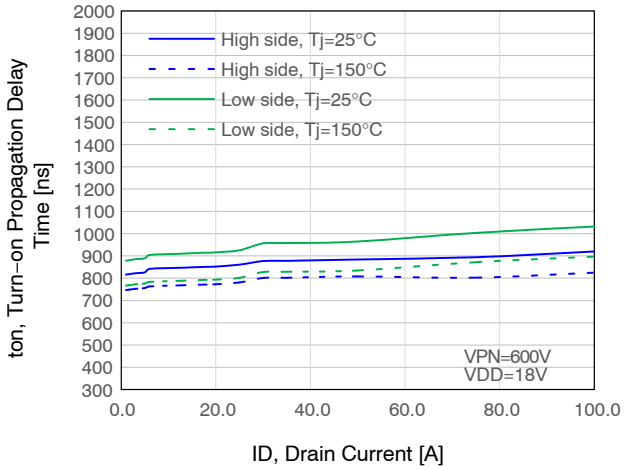


Figure 19. Typ. Turn−on Propagation Delay Time

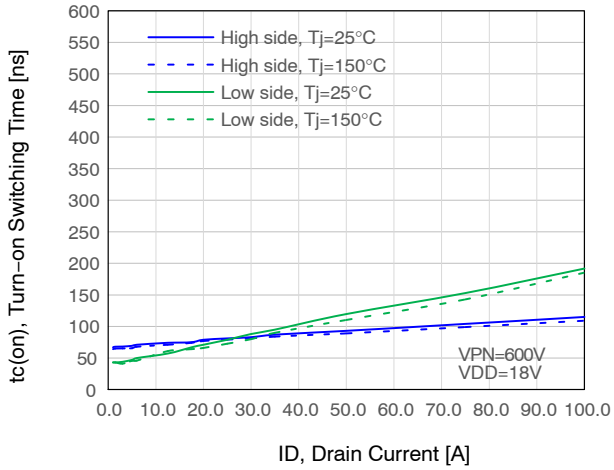


Figure 20. Typ. Turn−on Switching Time

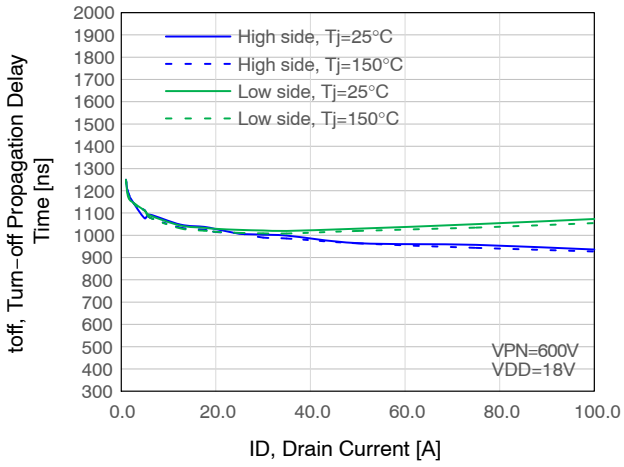


Figure 21. Typ. Turn off Propagation Delay Time

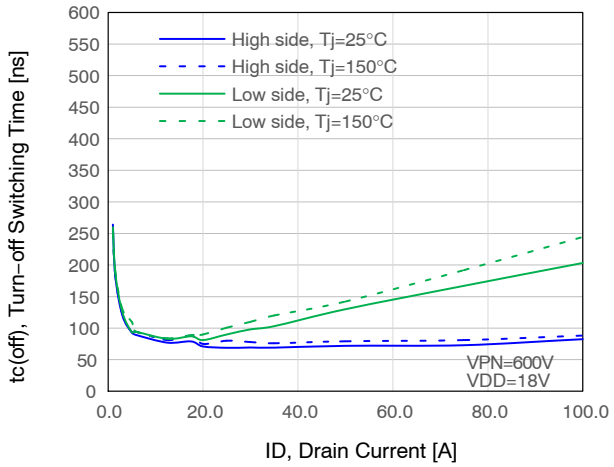


Figure 22. Typ. Turn off Switching Time

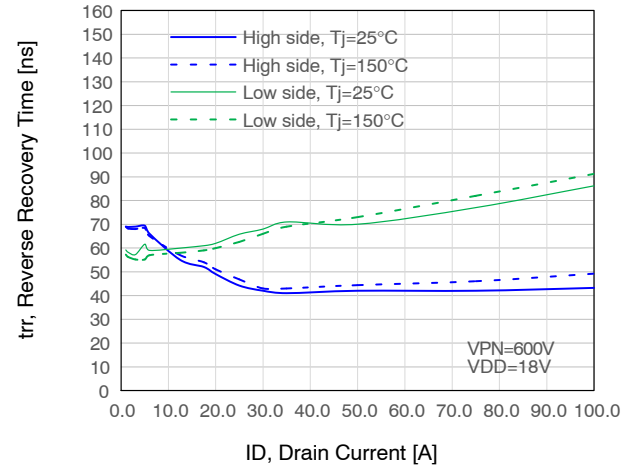


Figure 23. Typ. Reverse Recovery Time

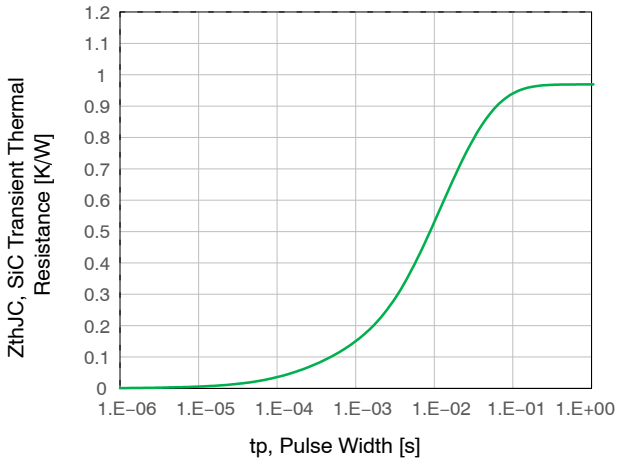


Figure 24. MOSFET Transient Thermal Resistance

TURN−ON/OFF SWITCHING WAVEFORM

Switching Condition: VPN = 600 V, VDD = 18 V, Tj = 25°C, Id = 50 A.

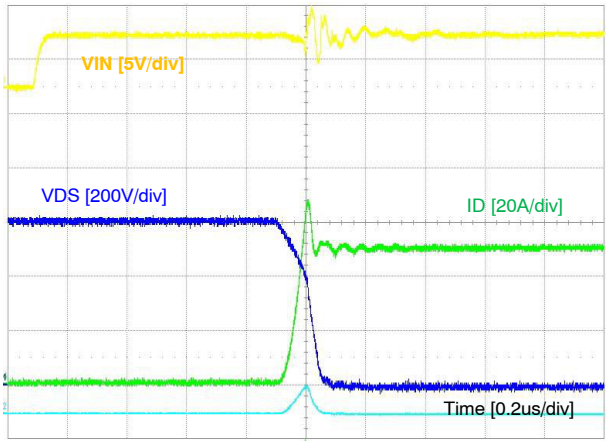


Figure 25. Turn−on Switching Waveform

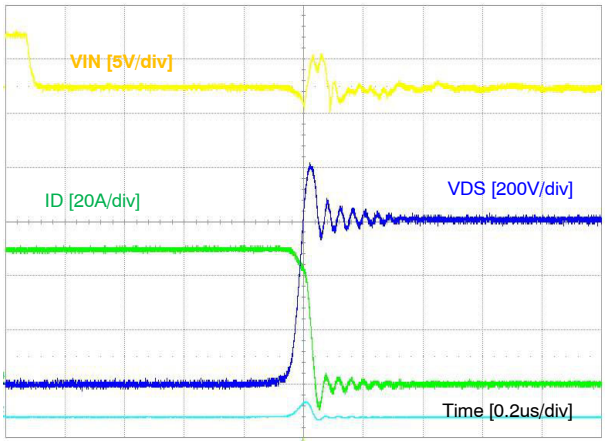


Figure 26. Turn−off Switching Waveform

Switching Condition: VPN = 600 V, VDD = 18 V, Tj = 150°C, Id = 50 A.

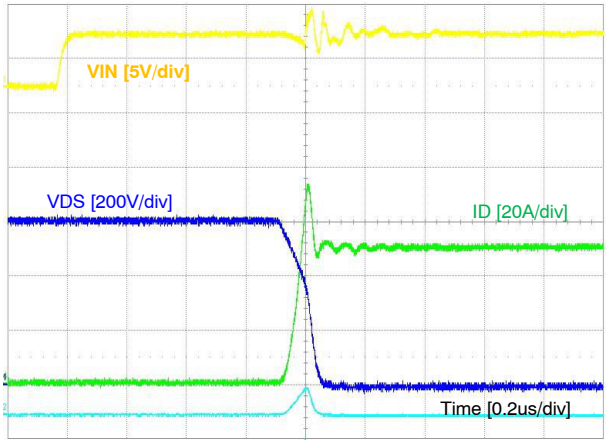


Figure 27. Turn−on Switching Waveform

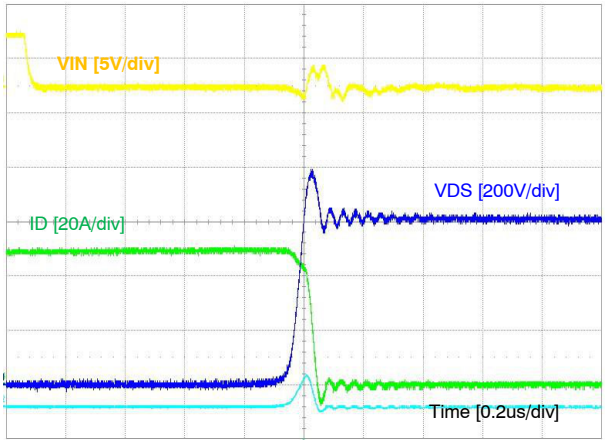
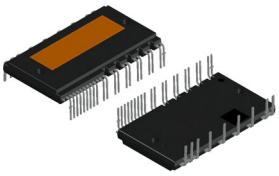


Figure 28. Turn−off Switching Waveform



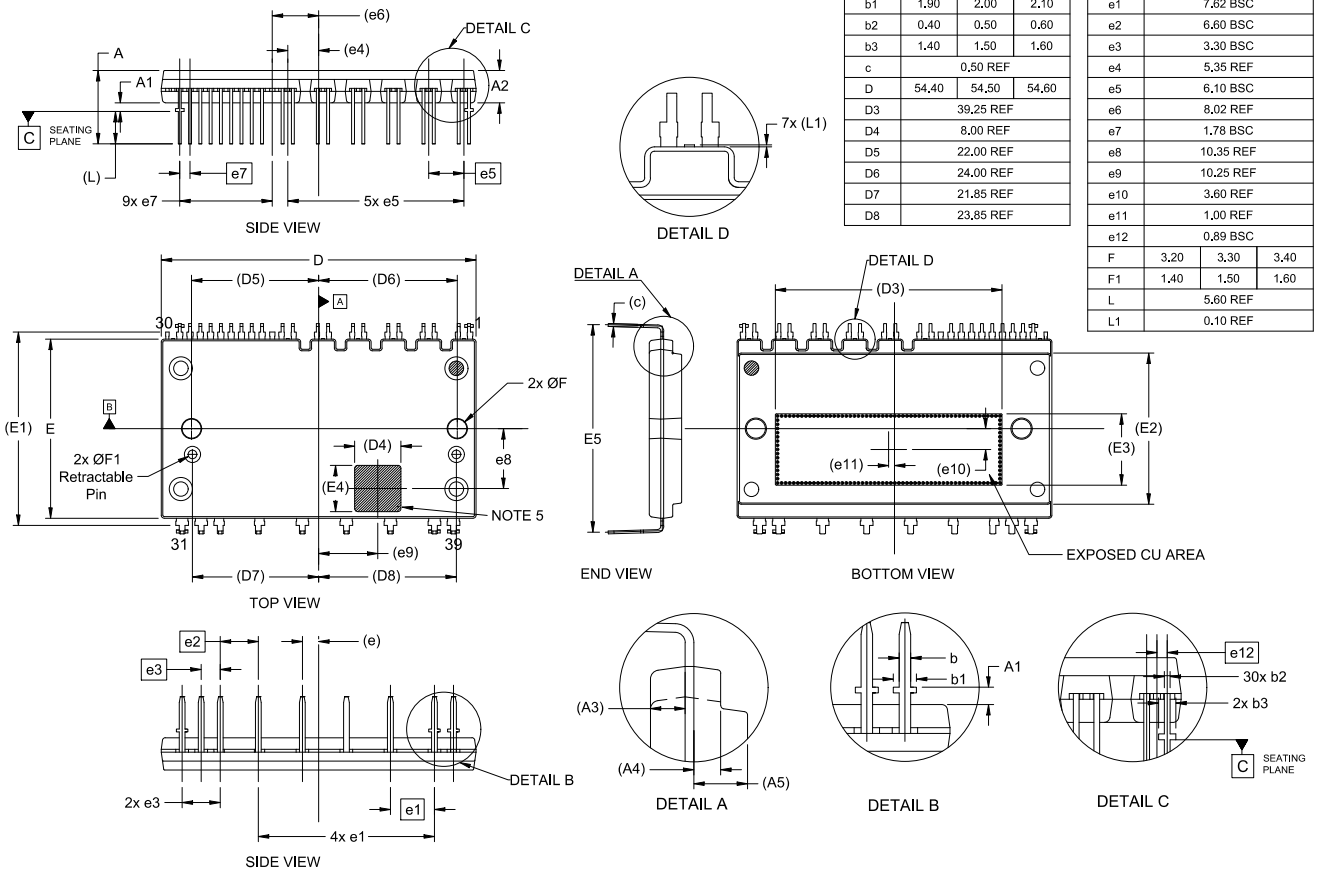
DIP39, 54.50x31.00x5.60, 1.78P
CASE MODGC
ISSUE B

DATE 21 DEC 2023

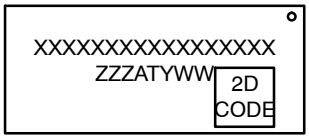
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP
4. POSITION OF THE LEAD IS DETERMINED AT THE BASE OF THE LEAD WHERE IT EXITS THE PACKAGE BODY
5. AREA FOR 2D BAR CODE
6. SHORTENED/CUT PINS ARE 2,5,8,11,14,17,19,29 AND 30

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	12.20	12.7	13.2
A1	1.00	1.50	2.00
A2	5.50	5.60	5.70
A3		2.00 REF	
A4		1.55 REF	
A5		3.10 REF	
b	0.90	1.00	1.10
b1	1.90	2.00	2.10
b2	0.40	0.50	0.60
b3	1.40	1.50	1.60
c		0.50 REF	
D	54.40	54.50	54.60
D3		39.25 REF	
D4		8.00 REF	
D5		22.00 REF	
D6		24.00 REF	
D7		21.85 REF	
D8		23.85 REF	

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E	30.90	31.00	31.10
E1		33.50 REF	
E2		26.14 REF	
E3		12.35 REF	
E4		8.00 REF	
E5	35.40	35.90	36.40
e		2.81 REF	
e1		7.62 BSC	
e2		6.60 BSC	
e3		3.30 BSC	
e4		5.35 REF	
e5		6.10 BSC	
e6		8.02 REF	
e7		1.78 BSC	
e8		10.35 REF	
e9		10.25 REF	
e10		3.60 REF	
e11		1.00 REF	
e12		0.89 BSC	
F	3.20	3.30	3.40
F1	1.40	1.50	1.60
L		5.60 REF	
L1		0.10 REF	



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
ZZZ = Assembly Lot Code
AT = Assembly & Test Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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