Automotive Power Over Coax Power Management IC for Safety Camera

NCV92310

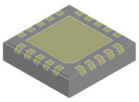
The NCV92310 is part of the **onsemi** image sensor power management IC (PMIC) family. It is optimized to supply power over coax (POC) automotive application sub−systems such as rear, front and surround view cameras. This NCV92310 integrates one power over coax DCDC converter, 2 high efficiency (1 A and 500 mA) Step−down DCDC converters with DVS (Dynamic Voltage Scale) and 1 low dropout (LDO) voltage regulators in a 3.5x3.5 mm QFNW20 package.

Features

- 1 Power Over Coax DCDC Converter (2.15 MHz, 2.2 µH/10 µF, 1.2 A)
  - Programmable Output Voltage from 2.8 V to 5.0 V by 100 mV Steps
- 1 DCDC Converters (2.15 MHz, 1 µH/10 µF, 1 A)
  - Programmable Output Voltage from 0.6 V to 2.175 V by 25 mV Steps
- 1 DCDC Converters (2.15 MHz, 1 µH/10 µF, 500 mA)
  - Programmable Output Voltage from 0.6 V to 2.175 V by 25 mV Steps
- 1 Low Noise − Low Drop Out Regulator (2.2 µF, 300 mA)
  - Programmable Output Voltage from 2.6 V to 3.3 V by 100 mV Steps
  - 50 µVrms Typical Low Output Noise (Vout = 2.8 V, 10 Hz to 100 kHz)
- Control
  - 400 kHz / 1 MHz I^2C Compatible
  - I^2C Enable Control Bits
  - /RST and Interrupt Output Pin
  - Customizable Power Up / Down Sequence with Soft Start
- Extended Input Voltage Range from 4.6 V to 18 V
- Footprint: 3.5x3.5 mm QFNW−20 0.5 mm Pitch

Applications

- Power Over Coax POL Supply
- Automotive ADAS Camera Modules
- Industrial Camera Modules

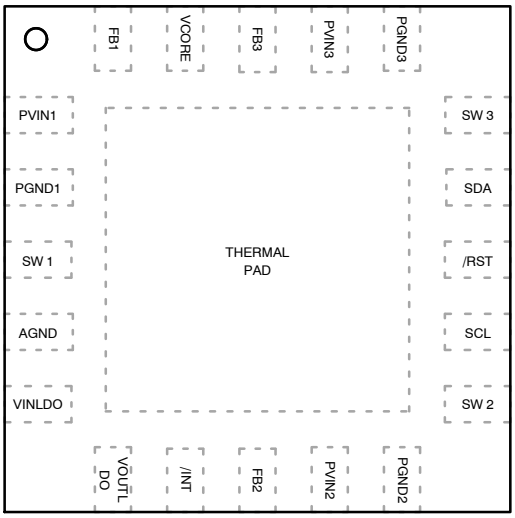


QFNW20 3.5x3.5, 0.5P
CASE 484AV

MARKING DIAGRAM

NCV92310AB	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week

PIN CONNECTIONS



(Top View)
20−Pins 3.5x3.5 0.50 mm pitch DFN

ORDERING INFORMATION

See detailed ordering and shipping information on page 59 of this data sheet.

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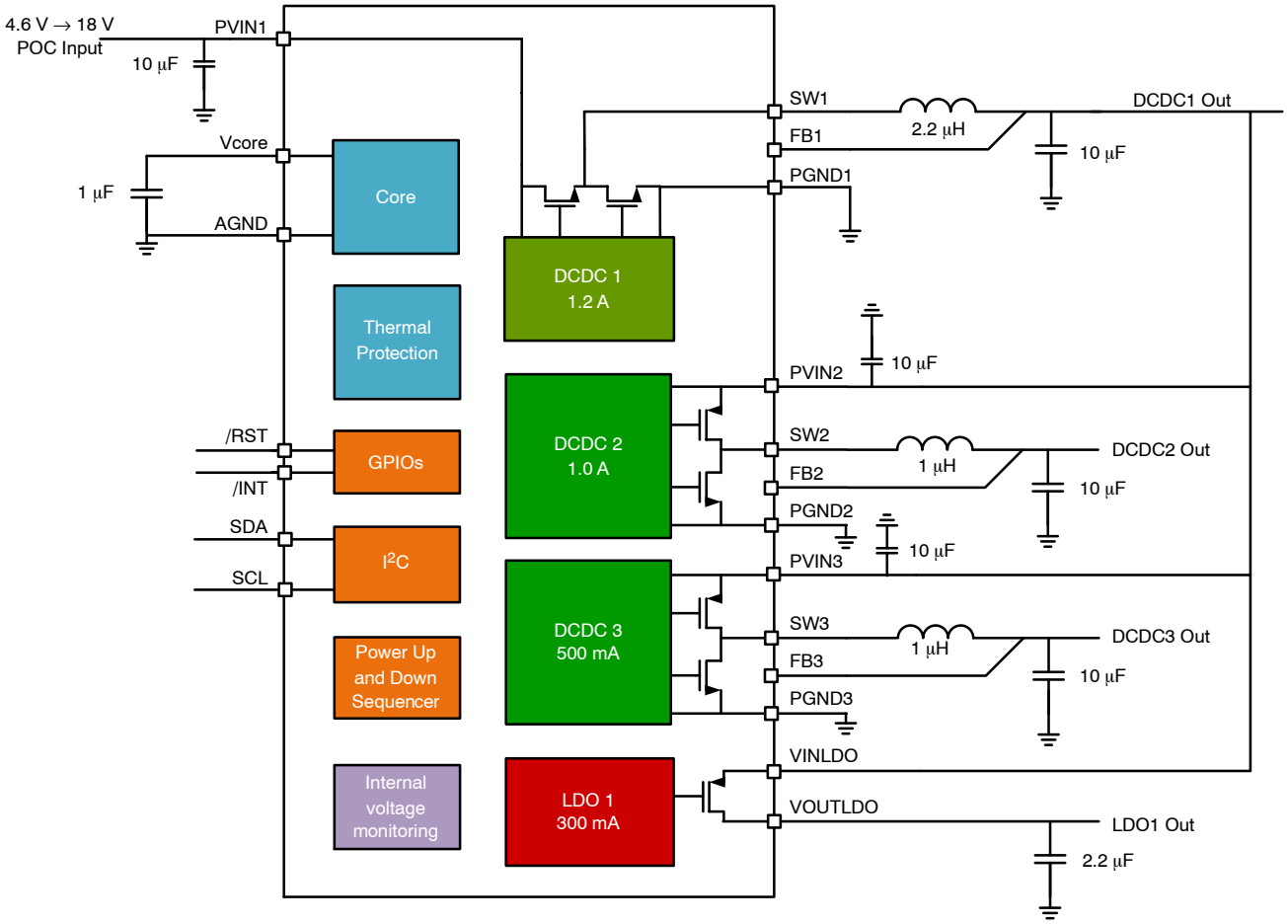

Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

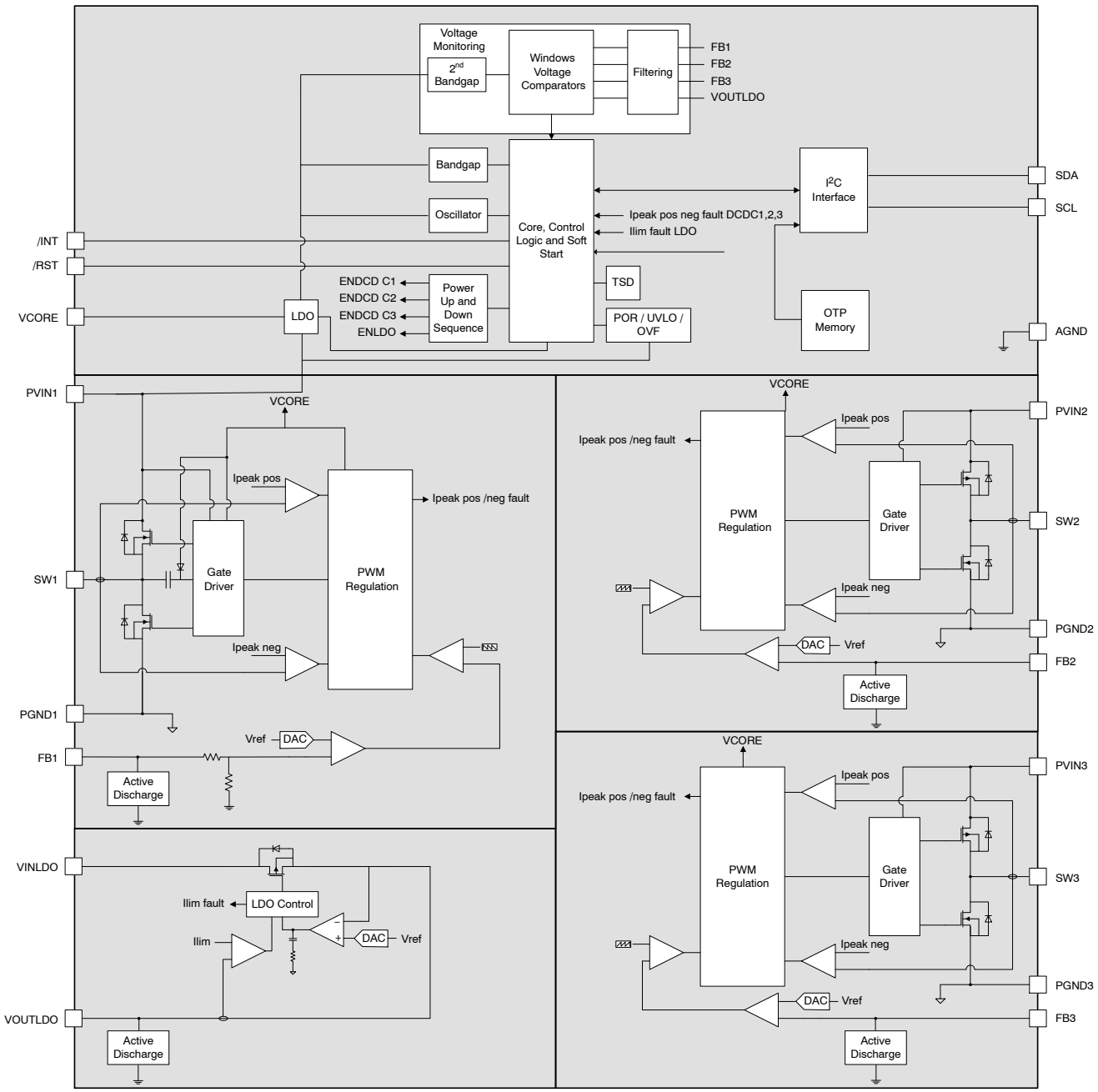

Figure 2. Simplified Block Diagram

PIN OUT DESCRIPTION

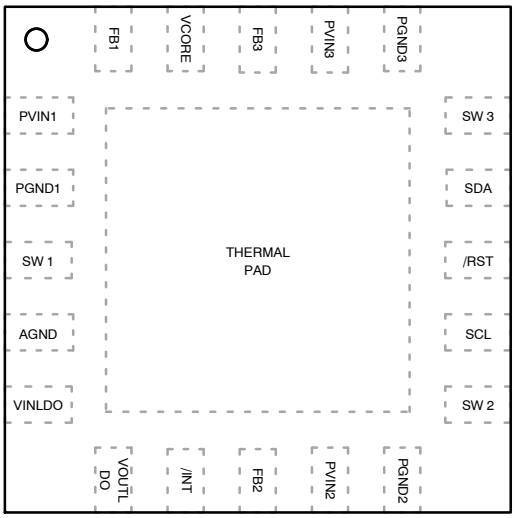

Figure 3. Pin Out (Top view)

PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
GENERAL			
19	VCORE	Analog Output	Reference voltage. A 1 μF ceramic capacitor (220 nF minimum) must bypass this pin to ground.
4	AGND	Analog Ground	Analog Ground. Analog and digital modules ground. Must be connected to the system ground.
7	/INT	Digital Output	Interrupt push−pull output.
13	/RST	Digital Output	Reset push−pull output.
12	SCL	Digital Input	I^2C interface Clock
14	SDA	Digital Input	I^2C interface Data
21	PAD	Exposed Pad	Exposed Pad. Must be soldered to system ground to achieve power dissipation performances. This pin is internally unconnected.
PoC DC−DC CONVERTERS			
1	PVIN1	Power Input	DCDC1 and Core Power Supply. This pin must be decoupled to ground by a 10 μF ceramic capacitor. This capacitor should be placed as close as possible to this pin.
3	SW1	Power Output	DCDC1 Switch Power. This pin connects the power transistors to one end of the inductor. Typical application uses 2.2 μH inductor; refer to Application section for more information.
20	FB1	Analog Input	DCDC1 Feedback Voltage. This pin is the input to the error amplifier and must be connected to the output capacitor.
2	PGND1	Power Ground	DCDC Power Ground. This pin is the power ground and carries the high switching current. A high quality ground must be provided to prevent noise spikes. A local ground plane is recommended to avoid high−density current flow in a limited PCB track.
1 A LOW VOLTAGE DC−DC CONVERTERS			
9	PVIN2	Power Input	DCDC2 Power Supply. This pin must be decoupled to ground by a 10 μF ceramic capacitor. This capacitor should be placed as close as possible to this pin.
11	SW2	Power Output	DCDC2 Switch Power. This pin connects the power transistors to one end of the inductor. Typical application uses 1.0 μH inductor; refer to Application section for more information.
8	FB2	Analog Input	DCDC2 Feedback Voltage. This pin is the input to the error amplifier and must be connected to the output capacitor.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Type	Description
1 A LOW VOLTAGE DC−DC CONVERTERS			
10	PGND2	Power Ground	DCDC2 Power Ground. This pin is the power ground and carries the high switching current. A high quality ground must be provided to prevent noise spikes. A local ground plane is recommended to avoid high−density current flow in a limited PCB track.
500 mA LOW VOLTAGE DC−DC CONVERTERS			
17	PVIN3	Power Input	DCDC3 Power Supply. This pin must be decoupled to ground by a 10 μF ceramic capacitor. This capacitor should be placed as close as possible to this pin.
15	SW3	Power Output	DCDC3 Switch Power. This pin connects the power transistors to one end of the inductor. Typical application uses 1.0 μH inductor; refer to Application section for more information.
18	FB3	Analog Input	DCDC3 Feedback Voltage. This pin is the input to the error amplifier and must be connected to the output capacitor.
16	PGND3	Power Ground	DCDC3 Power Ground. This pin is the power ground and carries the high switching current. A high quality ground must be provided to prevent noise spikes. A local ground plane is recommended to avoid high−density current flow in a limited PCB track.
LDO REGULATORS			
5	VINLDO	Power Input	LDO Power Supply
6	VOUTLDO	Power Output	LDO Output Power. This pin requires a 2.2 μF decoupling capacitor.

MAXIMUM RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
VP1−DC	Power Pins DC Non Switching: PVIN1, SW1 (Note 1)	−0.3	−	20	V
VP2−DC	Power Pins DC Non Switching: PVIN2, PVIN3, SW2, SW3 (Note 1)	−0.3	−	6.0	V
VA1−DC	Analog Pins DC Non Switching: FB2, FB3 (Note 1)	−0.3	−	V_{CORE}	V
VA2−DC	Analog Pins DC Non Switching: VCORE, FB1, VINLDO, VOUTLDO (Note 1)	−0.3	−	6.0	V
VA3−DC	Analog Pins DC Non Switching: VOUTLDO (Note 1)	−0.3	−	V_{INLDO}	V
VP1−TR	Between PVIN1−PGND1 Pins, Transient 3 ns − 2.15 MHz (Note 1)	−0.3	−	24	V
VP2−TR	Between PVIN2−PGND2 and PVIN3−PGND3 Pins, Transient 3 ns − 2.15 MHz (Note 1)	−0.3	−	7.0	V
VDG1	Digital Pins: SDA, SCL, /INT (Note 1)	−0.3	−	6.0	V
VDG2	Digital Pins: /RST (Note 1)	−0.3	−	V_{CORE}	V
HBM	ESD Withstand Voltage (Human Body Model) (Note 2)	500	−	−	V
CDM_CORNER	ESD Withstand Voltage (CDM) PVIN1, VINLDO, VOUTLDO, SW2, SW3, FB1 (Note 2)	750	−	−	V
CDM	ESD Withstand Voltage (CDM) All Others Pins than Corners (Note 2)	500	−	−	V
I_{LU}	Latch Up Current (Note 3)	−	100	−	mA
T_{STG}	Storage Temperature Range	−65	−	150	°C
T_{JMAX}	Junction Temperature Range	−40	−	170	°C
MSL	Moisture Sensitivity (Note 4)	−	Level1	−	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series contains ESD protection and passes the following ratings:
   Human Body Model (HBM) ±500 V per JEDEC standard: JESD22−A114.
   Charged Device Model (CDM) 750 V (corner pins) and 500 V (others pins) per JEDEC standard: JESD22−C101 Class IV.
3. Latch up Current per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
P_{VIN1_RANGE}	Power Input Supply	4.6	9	18	V
V_{VIN_RANGE}	Power Input Supply	2.8	–	5.5	V
L_{OUT1}	Inductor for the PoC DC to DC Converter (Note 5)	–	2.2	–	μH
L_{OUT2}	Inductor for the 1 A LV DC to DC Converter (Note 5)	–	1.0	–	μH
L_{OUT3}	Inductor for the 500 mA LV DC to DC Converter (Note 5)	–	1.0	–	μH
C_{CORE}	Vcore Pin Capacitor (Note 5)	0.120*	1	–	μF
C_{PVIN1}	Input Capacitor for the PoC DC to DC Converter (Note 5)	3*	10**	–	μF
C_{PVIN2}	Input Capacitor for the 1 A LV DC to DC Converter (Note 5)	5*	10**	–	μF
C_{PVIN3}	Input Capacitor for the 500 mA LV DC to DC Converter (Note 5)	5*	10**	–	μF
$C_{VINLDO1}$	Input Capacitor for the Internal LDO V_{INLDO} Connected to the DCDC1 Output (Note 5)	–	0**	–	μF
$C_{VINLDO2}$	Input Capacitor for the Internal LDO V_{INLDO} Connected to an External Supply (Note 5)	1**	2.2**	–	μF
C_{OUT1}	Output Capacitor for PoC DC to DC Converter (Note 5)	6.4*	10**	100**	μF
C_{OUT2}	Output Capacitor for the 1 A LV DC to DC Converter (Note 5)	5*	10**	100**	μF
C_{OUT3}	Output Capacitor for 500 mA LV DC to DC Converter (Note 5)	5*	10**	100**	μF
C_{OUTLDO}	Output Capacitor for the Internal LDO (Note 5)	1.65*	2.2**	47**	μF
T_J	Junction Temperature Range (Note 6)	–40	25	+150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
* derated value.
** nominal value.
5. Including de−ratings (Refer to the Application Information section of this document for further details)
6. The thermal shutdown set to 170°C (typical) avoids potential irreversible damage on the device due to power dissipation.
7. The RθJA is dependent of the PCB heat dissipation. Board used to drive this data was a NCV92100EVB board.
8. The maximum power dissipation (PD) is dependent by input voltage, maximum output current, pcb stack up and layout, and external components selected.

THERMAL INFORMATION

Symbol	Parameter	JEDEC JESD51−3 (Calculated)	Demo Board (Measured)	Unit
$\theta_{J-C\ TOP}$	Thermal Resistance Junction to Case Top Resistance (Note 9)	27.6	–	°C/W
θ_{JB}	Thermal Resistance Junction to Bottom Top Resistance (Note 10)	1.6	–	°C/W
θ_{JA}	Thermal Resistance Junction to Ambient QFNW20 on Demo−board (Note 11)	31	35	°C/W

9. Calculated with infinite heatsink affixed to case top without any board present.
10. Calculated with infinite heatsink affixed to case bottom without any board present.
11. The RθJA is dependent of the PCB heat dissipation. Board used to drive this data was a NCV92100EVB board.

ELECTRICAL CHARACTERISTICS (Refer to the Application Information section of this data sheet for more details. Min and Max Limits apply for T_J = −40°C to +150°C, V_{IN} range (PVIN_RANGE and VIN_RANGE) and default configuration, unless otherwise specified. Typical values are referenced to T_J = +25°C, V_{IN} = range and default configuration, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT: PIN VIN					
I_Q	Operating Quiescent Current, No Load Vin = 9 V, Default Configuration	–	13	–	mA
INTERNAL VOLTAGE REFERENCE					
V_{CORE}	Internal Voltage Reference for Core Supply	4.37	4.8	4.9	V
DCDC1 (PoC DCDC CONVERTER)					
V_{OUT1}	Output Voltage Accuracy Vin Range, Iout Range	−1.5	–	+1.5	%
$V_{OUT1\_33\_100mA}$	Default Output Voltage Vin = 9 V, Iout = 100 mA	3.2505	3.3	3.3495	V
D_{MAX1}	Maximum Duty Cycle	–	92	–	%
DC_{LOAD1}	Load Regulation, Iout from 100 mA to 1 A	–	0.05	–	%/A
DC_{LINE1}	Line Regulation, Vin from 5 V to 18 V, Iout = 100 mA	–	0.001	–	%/V
$I_{OUTMAX1}$	Output Current Range (Note 12)	1.2	–	–	A
I_{LIMP1}	Output Peak Current High Side Switch (Note 12)	1.5	1.8	2.1	A
I_{LIMN1}	Output Peak Current Low Side Switch (Note 12)	–	1	–	A
R_{ON_H1}	High−Side MOSFET ON Resistance	–	385	–	mΩ
R_{ON_L1}	Low−Side MOSFET ON Resistance	–	250	–	mΩ
R_{DIS1}	Internal Active Output Discharge, from FB to PGND Vout = 3.3 V	–	80	–	Ω
DCDC2 (1 A LV DCDC CONVERTER)					
V_{OUT21}	Output Voltage Accuracy Vin Range, Vout Range, Iout Range	−1	–	+1	%
$V_{OUT2\_12\_100mA}$	Default Output Voltage Vin = 3.3 V, Iout = 100 mA	1.188	1.2	1.212	V
DC_{LOAD2}	Load Regulation, Iout from 100 mA to 1 A	–	0.05	–	%/A
DC_{LINE2}	Line Regulation, Vin from 2.8 V to 5.5 V, Iout = 100 mA	–	0.001	–	%/V
$I_{OUTMAX2}$	Output Current Range (Note 12)	1	–	–	A
I_{LIMP2}	Output Peak Current High Side Switch P_{VIN2} = 3.3 V (Note 12)	1.65	2.0	2.35	A
I_{LIMN2}	Output Peak Current Low Side Switch P_{VIN2} = 3.3 V (Note 12)	–	1.2	–	A
R_{ON_H2}	High−Side MOSFET ON Resistance	–	120	–	mΩ
R_{ON_L2}	Low−Side MOSFET ON Resistance	–	90	–	mΩ
R_{DIS2}	Internal Active Output Discharge, from FB to PGND Vout = 1.2 V	–	100	–	Ω
DCDC3 (500 mA LV DCDC CONVERTER)					
V_{OUT31}	Output Voltage Accuracy Vin Range, Vout Range, Iout Range	−1	–	+1	%
$V_{OUT3\_18\_100mA}$	Default Output Voltage Vin = 3.3 V, Iout = 100 mA	1.782	1.8	1.818	V
DC_{LOAD3}	Load Regulation, Iout from 100 mA to 500 mA	–	0.05	–	%/A
DC_{LINE3}	Line Regulation, Vin from 2.8 V to 5.5 V, Iout = 100 mA	–	0.001	–	%/V
$I_{OUTMAX3}$	Output Current Range (Note 12)	0.5	–	–	A
I_{LIMP3}	Output Peak Current High Side Switch P_{VIN3} = 3.3 V (Note 12)	1.35	1.7	2.05	A
I_{LIMN3}	Output Peak Current Low Side Switch P_{VIN3} = 3.3 V (Note 12)	–	1.2	–	A
R_{ON_H3}	High−Side MOSFET ON Resistance	–	220	–	mΩ

ELECTRICAL CHARACTERISTICS (Refer to the Application Information section of this data sheet for more details. Min and Max Limits apply for T_J = −40°C to +150°C, V_{IN} range (PVIN_RANGE and VIN_RANGE) and default configuration, unless otherwise specified. Typical values are referenced to T_J = +25°C, V_{IN} = range and default configuration, unless otherwise specified.) (continued)

Symbol	Parameter	Min	Typ	Max	Unit
DCDC3 (500 mA LV DCDC CONVERTER)					
R_{ON_L3}	Low−Side MOSFET ON Resistance	–	145	–	mΩ
R_{DIS3}	Internal Active Output Discharge, from FB to PGND Vout = 1.8 V	–	100	–	Ω
LOW DROPOUT REGULATOR					
I_{OUTLDO_1}	Maximum Output Current, V_{IN} Range, $V_{OUT} \le V_{IN} - 200$ mV (Note 12)	300	–	–	mA
$I_{LIMITLDO}$	Current Limit, V_{INLDO} = 3.1 V, V_{OUTLDO} = 2.8 V	350	–	620	mA
$\Delta V_{OUT\_LDO\_1}$	Output Voltage Accuracy, V_{IN} = 3.3 V, V_{OUT} = 2.8 V No Load	−1.0	VNOM	+1.0	%
$\Delta V_{OUT\_LDO\_2}$	Output Voltage Accuracy, V_{INLDO} Range, I_{OUTLDO} Range	−1.0	VNOM	+1.0	%
$DC_{LOADLDO}$	Load Regulation, I_{OUT} = 0 mA to 200 mA	–	0.04	–	%
$DC_{LINELDO}$	Line Regulation, V_{INLDO} = 3.1 V to 5.5 V I_{OUTLDO} = 200 mA	–	0.04	–	%
V_{DROP}	Dropout Voltage, VOUT = 2.8 V, I_{OUT} = 300 mA	80	110	210	mV
$PSRR_{\_1k}$	Ripple Rejection, F = 1 kHz V_{INLDO} = 3.3 V, V_{OUTLDO} = 2.8 V, I_{OUTLDO} = 100 mA	–	−80	–	dB
$PSRR_{\_10k}$	Ripple Rejection, F = 10 kHz V_{INLDO} = 3.3 V, V_{OUTLDO} = 2.8V, I_{OUTLDO} = 100 mA	–	−75	–	dB
$PSRR_{\_100k}$	Ripple Rejection, F = 100 kHz V_{INLDO} = 3.3 V, V_{OUTLDO} = 2.8V, I_{OUTLDO} = 100 mA	–	−60	–	dB
$PSRR_{\_1M}$	Ripple Rejection, F = 1 MHz V_{INLDO} = 3.3 V, V_{OUTLDO} = 2.8V, I_{OUTLDO} = 100 mA	–	−35	–	dB
Noise	Output Noise, 10 Hz → 100 kHz V_{OUTLDO} = 2.8 V	–	34	–	μV
R_{DISLDO}	LDO Active Output Discharge, V_{OUT} = 2.8 V	–	105	–	Ω
UVLO AND OVLO					
V_{INUV-}	V_{IN} UVLO Falling Threshold, P_{VIN1} Pin, Default Setting	5	5.1	–	V
V_{INUV+}	V_{IN} UVLO Rising Threshold, P_{VIN1} Pin, Default Setting		6.8	7	V
V_{INUV-_RANGE}	V_{IN} UVLO Falling Threshold, P_{VIN1} Pin, Programmability Range (See Table x)	4.35	–	7	V
V_{INUV+_RANGE}	V_{IN} UVLO Rising Threshold, P_{VIN1} Pin, Programmability Range (See Table x)	4.5	–	8	V
V_{INOV+}	V_{IN} OVF Rising Threshold, P_{VIN1} Pin	18	18.3	18.6	V
$V_{INOVHYST}$	V_{IN} OVF Hysteresis	–	204	–	mV
$V_{INOVDBN}$	V_{IN} OVF Debounce Time, P_{VIN1} Pin	–	10	–	μs
WINDOWS VOLTAGE MONITORING					
V_L	Undervoltage Detection Threshold, Programmability (3 Bits)	−10	–	−3	%
V_H	Overvoltage Detection Threshold, Programmability (3 Bits)	3	–	10	%
V_{LH}	Undervoltage Detection Hysteresis, $V_{OUT} \le 2.2$ V	–	4.5	7.6	mV
V_{HH}	Overvoltage Detection Hysteresis, $V_{OUT} \le 2.2$ V	–	4.5	7.6	mV
V_{LH_SC}	Undervoltage Detection Hysteresis, $V_{OUT} > 2.2$ V	–	11.25	19	mV
V_{HH_SC}	Overvoltage Detection Hysteresis, $V_{OUT} > 2.2$ V	–	11.25	19	mV
D_{ACC1}	Detection Accuracy, 0.6 V ≤ V_{OUT} < 1 V	−10	–	10	mV
D_{ACC2}	Detection Accuracy, $V_{OUT} \ge 1$ V	−1	–	1	%
T_{L_R}	Undervoltage Detection Debounce Programmability, Rising Edge	32	–	256	μs

ELECTRICAL CHARACTERISTICS (Refer to the Application Information section of this data sheet for more details. Min and Max Limits apply for T_J = −40°C to +150°C, V_{IN} range (PVIN_RANGE and VIN_RANGE) and default configuration, unless otherwise specified. Typical values are referenced to T_J = +25°C, V_{IN} = range and default configuration, unless otherwise specified.) (continued)

Symbol	Parameter	Min	Typ	Max	Unit
WINDOWS VOLTAGE MONITORING					
T_{L_F}	Undervoltage Detection Debounce Programmability, Falling Edge	0	–	128	μs
T_{H_R}	Overvoltage Detection Debounce Programmability, Rising Edge	0	–	128	μs
T_{H_F}	Overvoltage Detection Debounce Programmability, Falling Edge	32	–	256	μs
$V_{DISABLE\_DCDC1}$	Disable Detection Threshold DCDC1	–	2000	–	mV
$V_{DISABLE\_DCDC2}$	Disable Detection Threshold DCDC2	–	600	–	mV
$V_{DISABLE\_DCDC3}$	Disable Detection Threshold DCDC3	–	600	–	mV
$V_{DISABLE\_LDO1}$	Disable Detection Threshold LDO1	–	100	–	mV
TURN ON TIME AND SOFT−START					
T_{SS}	Turn ON time, Default Setting, from PVIN1 to Power Up Sequence Start	–	5.12	–	ms
T_{SS1}	Soft−start Time DCDC1, Time from 10% to 90% of Output Voltage Target (Default Setting), Vout = 3.3 V	–	0.845	–	ms
T_{SS2}	Soft−start Time DCDC2, Time from 10% to 90% of Output Voltage Target (Default Setting), Vout = 1.2 V	–	0.31	–	ms
T_{SS3}	Soft−start Time DCDC3, Time from 10% to 90% of Output Voltage Target (Default Setting), Vout = 1.8 V	–	0.45	–	ms
T_{SS4}	Soft−start Time LDO, Time from 10% to 90% of Output Voltage Target (Default Setting), Vout = 2.8 V, COUT = 2.2 μF	–	1.45	–	ms
INTERNAL CLOCKS					
CLK_{SYSOSC}	Internal System Clock	1.86	2.00	2.14	MHz
F_{SW}	DCDC Switching Frequency	2	2.15	2.3	MHz
Φ_{DCDC2_DCDC1}	Phase Shift between DCDC2 and DCDC1	–	120	–	°
Φ_{DCDC3_DCDC1}	Phase Shift between DCDC3 and DCDC1	–	240	–	°
THERMAL SHUTDOWN					
T_{SD}	Thermal Shutdown	–	163	–	°C
T_{WNG}	Thermal Warning	–	152	–	°C
T_{WNGH}	Thermal Warning Hysteresis	–	10	–	°C
T_{PWNG}	Thermal Pre−Warning (Default)	–	138	–	°C
T_{PWNGH}	Thermal Pre−Warning Hysteresis (Default)	–	6	–	°C
T_{GATING}	Thermal Gating Threshold / Thermal Shutdown Low Threshold	–	125	–	°C
/RST AND /INT PINS (PUSH−PULL)					
V_{INT_L}	/INT Pin Low Voltage, I_{INT} = 3 mA	–	–	0.3	V
V_{INT_H1}	/INT Pin High Voltage, I_{INT} = −3 mA $V_{OUT} \geq$ 1.2 V	V_{OUT_DCDC3} x 0.65	–	–	V
V_{INT_H2}	/INT Pin High Voltage, I_{INT} = −3 mA V_{OUT} < 1.2 V	V_{OUT_DCDC3} − 0.45	–	–	V
V_{RST_L}	/RST Pin Low Voltage, I_{RST} = 3 mA	–	–	0.3	V
V_{RST_H1}	/RST Pin High Voltage, I_{RST} = −3 mA $V_{OUT} \geq$ 1.2 V	V_{OUT_DCDC3} x 0.65	–	–	V
V_{RST_H2}	/RST Pin High Voltage, I_{RST} = −3 mA V_{OUT} < 1.2 V	V_{OUT_DCDC3} − 0.45	–	–	V

ELECTRICAL CHARACTERISTICS (Refer to the Application Information section of this data sheet for more details. Min and Max Limits apply for T_J = −40°C to +150°C, V_{IN} range (PVIN_RANGE and VIN_RANGE) and default configuration, unless otherwise specified. Typical values are referenced to T_J = +25°C, V_{IN} = range and default configuration, unless otherwise specified.) (continued)

Symbol	Parameter	Min	Typ	Max	Unit
I²C INTERFACE					
V_{I2C_H}	SCL and SDA Input Logic High (Note 13, 14, 15)	1.15	–	–	V
V_{I2C_L}	SCL and SDA Input Logic Low (Note 16)	–	–	0.45	V
V_{SDAO_L}	SDA Output Active Low, Sink 15 mA (Note 17)	–	–	0.4	V
I_{SDAO_H}	SDA Output Open Drain Leakage, 5.5 V		–	500	nA
F_{I2C}	SCL Clock Frequency, 1.8 V Supplied I/O Rail (Note 13, 17, 18)	0	–	1	MHz
$I2C_{SS}$	Pulse Width of Spikes that Must Be Suppressed by the Pinout Filter (Note 19)	–	–	50	ns
C_{I2C}	SCL and SDA Input Pin Capacitance	–	5	–	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

12. Junction temperature must be maintained below 150°C. Output load current capability depends on the application thermal capability.
13. In support of Fast Mode Plus, 1.8 V supplied I/O rails and the related 100 mV of drop totaling 1.7 V minimum.
14. For any input voltage greater than the minimum value indicated the signal is guaranteed detected high.
15. I²C typical VIO 1.8 V to 3.3 V.
16. For any input voltage smaller than the maximum value indicated the signal is guaranteed detected low.
17. Fast Mode Plus fall time (tf) and rise time (tr) required (120 ns maximum).
18. I²C bus frequency may be adjusted depending on the actual operating voltage, pull−up resistance, bus capacitance (which could be up to 400 pF) and master GPIO driver strength.
19. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

TYPICAL OPERATING CHARACTERISTICS

(PV_{IN1} = 9 V (Unless otherwise noted). T_A = +25°C, DCDC2 = 1.20 V, DCDC2 = 1.3 V, LDO1 = 2.8 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μH (2016) − C_{DCDC} = 10 μF 0603 / X7T)

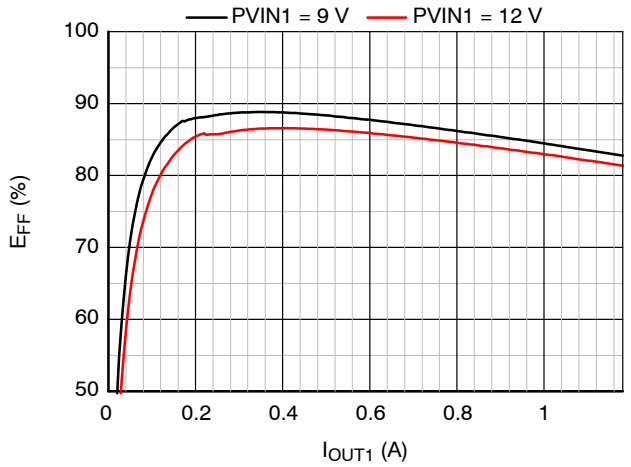

Figure 4. DCDC1 Efficiency vs. I_{LOAD} and V_{IN}, V_{OUT} = 3.30 V, TFM252012ALMA2R2 Inductor

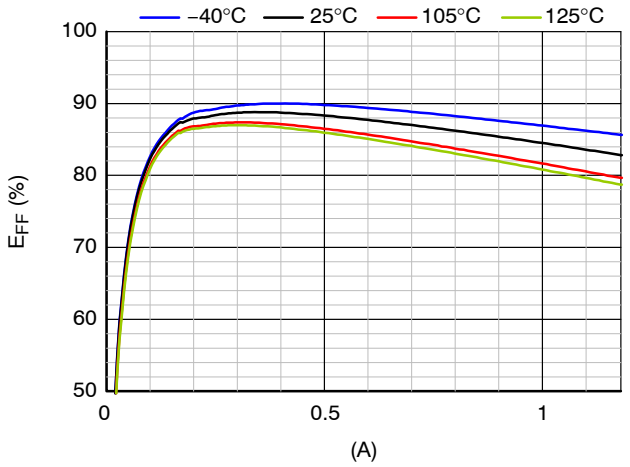

Figure 5. DCDC1 Efficiency Temperature V_{IN} = 9.0 V, V_{OUT} = 3.30 V, TFM252012ALMA2R2 Inductor

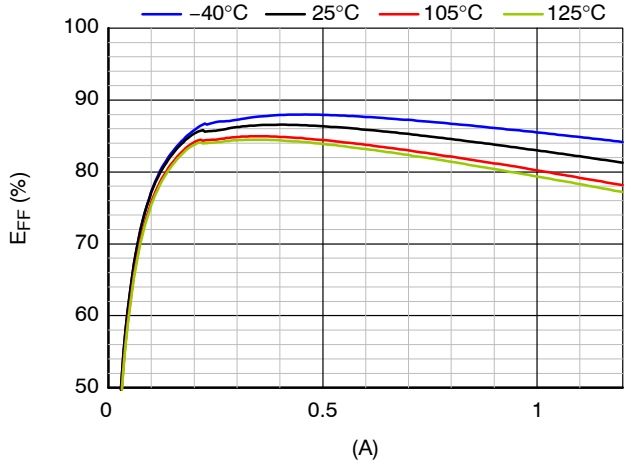

Figure 6. DCDC1 Efficiency Temperature V_{IN} = 12.0 V, V_{OUT} = 3.30 V, TFM252012ALMA2R2 Inductor

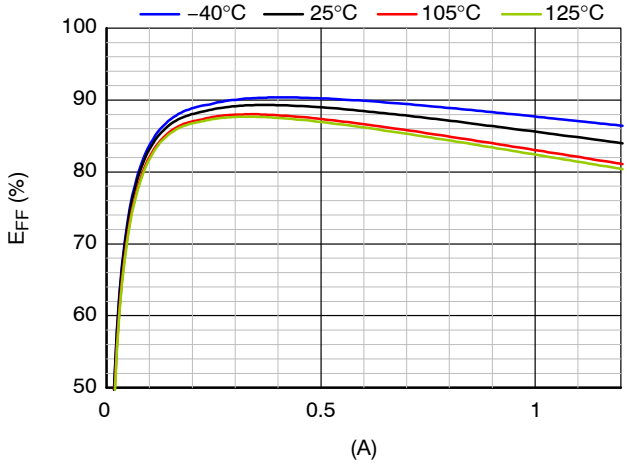

Figure 7. DCDC2 Efficiency vs. I_{LOAD} and Temperature V_{IN} = 3.3 V, V_{OUT} = 1.2 V, DFEMCAH2R2 Inductor

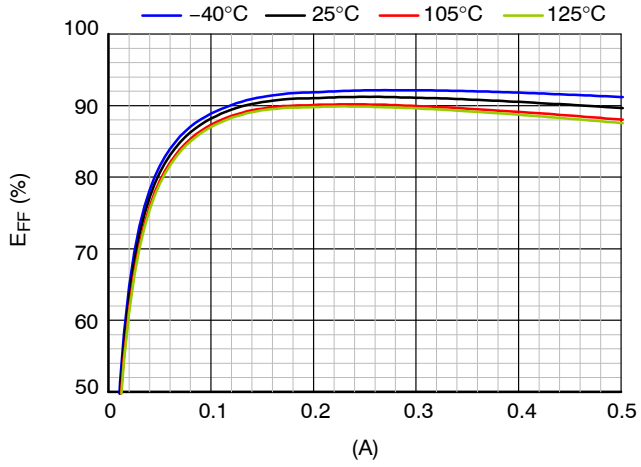

Figure 8. DCDC3 Efficiency vs. I_{LOAD} and Temperature V_{IN} = 3.3 V, V_{OUT} = 1.8 V, DFEMCAH2R2 Inductor

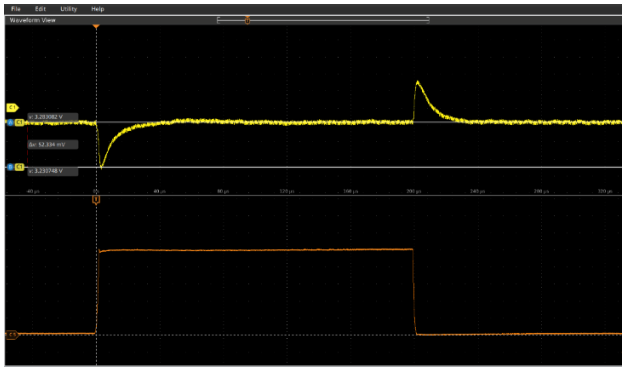

Figure 9. DCDC1 Load Transient VIN = 9 V, VOUT = 3.3 V, ILOAD from 10 mA to 1A

TYPICAL OPERATING CHARACTERISTICS

(PV_{IN1} = 9 V (Unless otherwise noted). T_A = +25°C, DCDC2 = 1.20 V, DCDC2 = 1.3 V, LDO1 = 2.8 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μH (2016) − C_{DCDC} = 10 μF 0603 / X7T) (Continued)

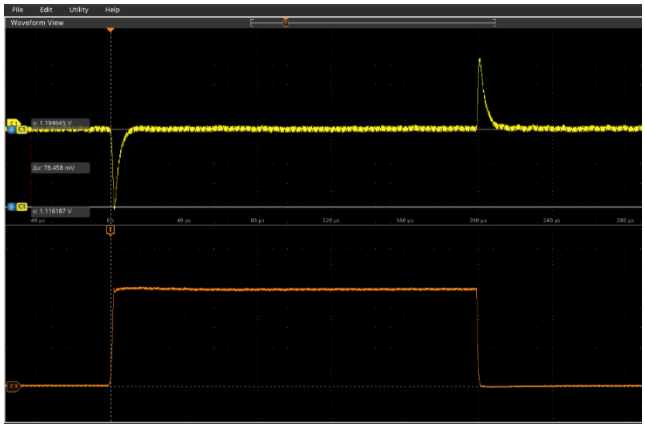

Figure 10. DCDC2 Load Transient
V_{IN} = 3.3 V, V_{OUT} = 1.2 V, I_{LOAD} from 10 mA to 1 A

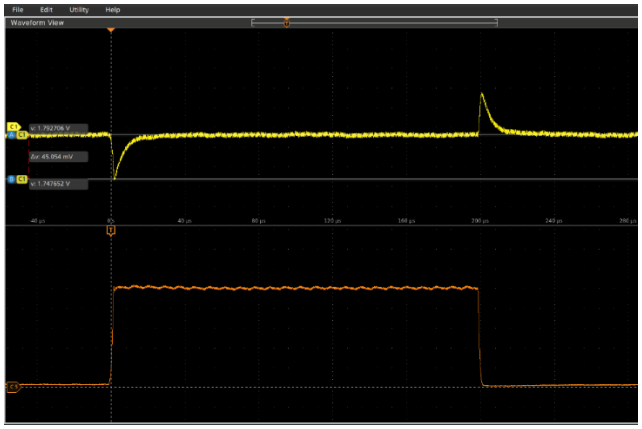

Figure 11. DCDC3 Load Transient
V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{LOAD} from 10 mA to 500 mA

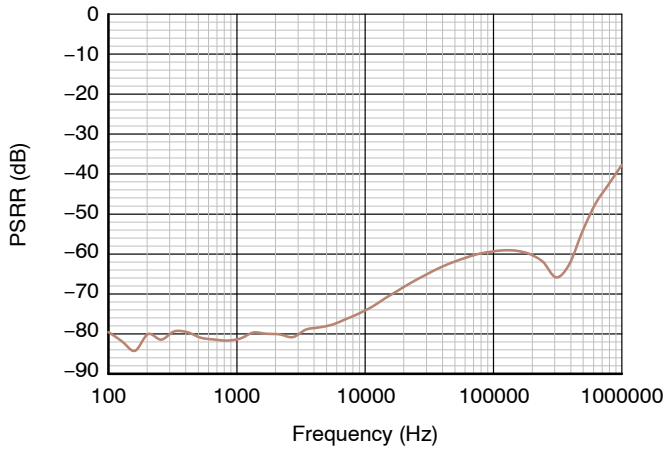

Figure 12. LDO1 PSRR
V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 100 mA

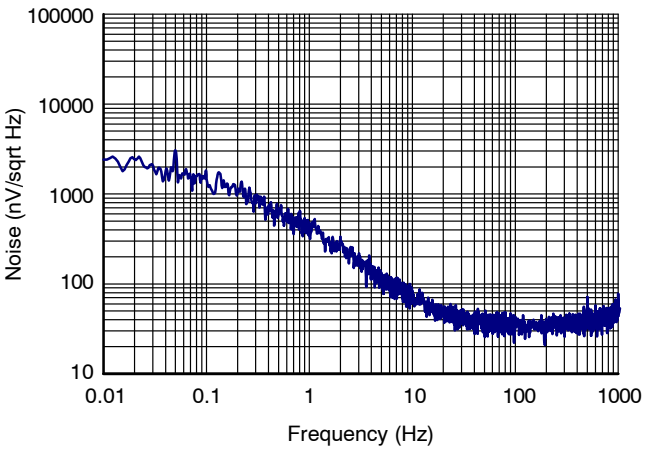

Figure 13. LDO Output Noise
V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 100 mA

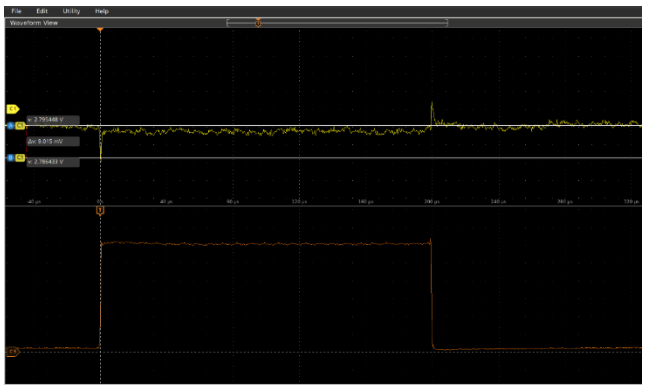

Figure 14. LDO1 Load Transient
V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{LOAD} from 10 mA to 300 mA

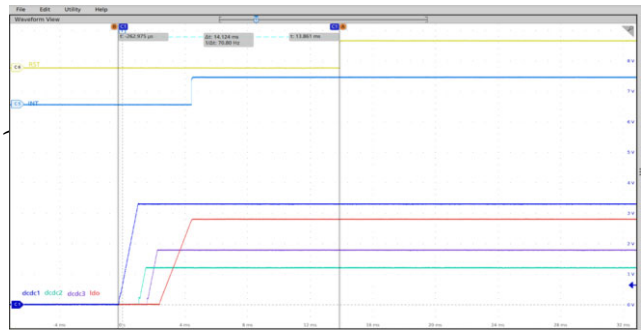

Figure 15. Power−up Sequence Example

DETAILED OPERATING DESCRIPTION

General

The NCV92310 is optimized to supply cameras of automotive Power over Coax applications.

It integrates one Power Over Coax switched mode DCDC converters, two low voltage switched mode DCDC converters and one low dropout linear regulator. The IC is widely programmable through an I^2C interface with a default setting provided by the internal OTP memory set during the manufacturing process. The core of the NCV92310 is supplied from PVIN1 from where a low voltage core voltage VCORE is derived. The VCORE supplies most of the on−chip analog and digital circuitry. PVIN1 can be supplied from a 5 V regulated source or connected directly to the filtered power over coax supply.

The output voltage range, current capabilities and performances of the switched mode DCDC converters are well suited to supply a camera module. For PWM operation, the converters run on a local 2.15 MHz. All the switching components are integrated including the compensation networks and synchronous rectifier. Only a small size inductor (2.2 μH for the PoC DCDC and 1 μH for the LV DCDCs) and 10 μF bypass capacitor are required for typical applications. Higher output capacitor value may be needed depending on the load transient requirement.

The low noise low dropout regulator can be used to supply the lower power rails in the application. The regulator is bypassed with a small size 2.2 μF capacitor. Higher output capacitor value may be needed depending on the load transient requirement.

The low voltage regulators (DCDC2, DCDC3, LDO1) each have their own input supply pin to be able to connect it either independently to the system supply rail or to the DCDC converter output, in the application. Like DCDC1, each converter and LDO is enabled smoothly with a controlled ramp up in order to avoid any inrush current.

All supply rails are monitored by on−chip voltage window monitors. The window size and detection speed are programmable. When a monitor is tripped, an interrupt is generated and shutdown scenarios can be engaged. The monitors are also used to verify if the order of the power up and power down sequences are respected. Both mechanisms are essential in reaching a high level of functional safety.

The overall operation of the NCV92310 PMIC is governed by a state machine that will handle the initialization of the IC and the built−in self−test, the fault states, and the different operating modes.

All regulators include an active output discharge which can be independently enabled / disabled by the appropriate settings in the DIS register (refer to the register definition section). However to prevent any disturbances on the power−up sequence, a quick active output discharge is done during the start−up sequence for all output channels.

DCDCs PWM Mode Operation

All internal DCDCs operate in PWM mode from a fixed clock and adapts its duty cycle to regulate the desired output voltage. In this mode, the inductor current is in CCM and the voltage is regulated by PWM. The internal low side switch operates as synchronous rectifier and is driven complementary to the high side switch. In CCM, the lower side switch in a synchronous converter provides a lower voltage drop than the diode in an asynchronous converter, which provides less loss and higher efficiency.

DCDCs Switching Clock and Spread Spectrum

Switching Clock of the 3 DCDCs operates at 2.15 MHz. To avoid a too high inrush current, a phase shift is applied for each DCDC converter (DCDC1: 0°, DCDC2: 120°, DCDC3: 240°)

In order to optimize the peak emission of the DC to DC converters switching frequency, a frequency spreading option allows to spread the switching frequency of the converters which can be useful in meeting system EMI requirements. This option, available with on chip internal oscillator, is factory programmable and can be changed thru I^2C.

NCV92310 integrates a random spread spectrum (16 frequencies) with OTPs and I^2C programmable tolerance (5% max and 10% max).

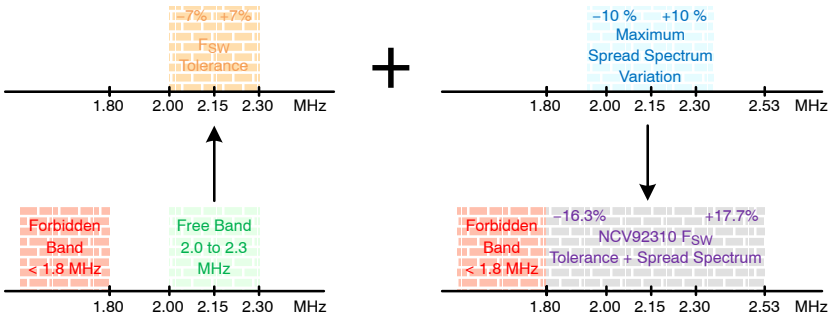

Figure 16. Tolerance + Spread Spectrum with Spread = 10% Max

Different spread spectrum modulations are available based on 16 frequency bins. By default, the triangular double peak modulation is used with OTPs and I²C programmable tolerance (±5% max, ±10% max). The frequency change can occur every n buck cycles (n is spread spectrum modulation divider from 1 to 128). Resulting modulation frequency is

$$F_M = \frac{F_{SW}}{n \times 32} \quad \text{(eq. 1)}$$

(with n is spread spectrum modulation divider)

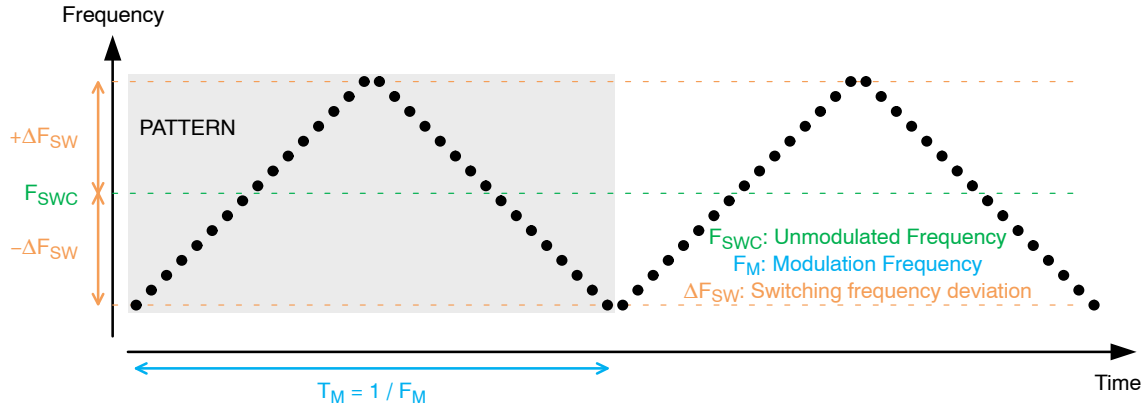

Figure 17. Tolerance + Spread Spectrum with Spread = 10% Max

Pseudorandom modulation with 16 bits pattern is also available.

Low Dropout Regulator

Internal LDO is a low noise, high PSRR and high bandwidth regulator intended to supply image sensor analog pixel input.

Its extended bandwidth allows best in class load transient performances, which helps improve image quality.

Internal LDO limit the output current at 90 mA worst case ($I_{LDO\_STARTUP}$) during the startup phase. LDO soft start setting and total output capacitor connected at the VOUTLDO is selected by the following equation:

$$Cout\_ldo\_max = Ildo\_startup \times \frac{\Delta t}{\Delta V} \quad \text{(eq. 2)}$$

If C_{OUT_LDO} exceed $C_{OUT\_LDO\_MAX}$, internal short circuit protection may be triggered.

Soft Start Time Setting

Soft start timing is set thru I²C and On Time Programmable internal memory.

Table 1. SOFT START SETTINGS

Buck Soft Start Time (ms)	LDO Soft Start Time (ms)
$0.64_{(ms/V)}$ x V_{OUT}	$1.28_{(ms/V)}$ x V_{OUT}
$0.32_{(ms/V)}$ x V_{OUT} (default)	$0.64_{(ms/V)}$ x V_{OUT} (default)
$0.16_{(ms/V)}$ x V_{OUT}	$0.32_{(ms/V)}$ x V_{OUT}
$0.08_{(ms/V)}$ x V_{OUT}	$0.16_{(ms/V)}$ x V_{OUT}

It allows limiting the inrush current at the input during the power−up sequence.

Regulator Stability

DCDC Regulators

DCDC1, DCDC2 and DCDC3 use a voltage mode architecture. Regulators stability depends on the output LC filter.

Each regulator embeds an OTP bit that allow managing the stability versus the total output capacitor value. With the default inductor value (DCDC1 = 2.2 µH, DCDC2 and DCDC3 = 1 µH), output capacitor range without derating is:

- 10 µF to 50 µF (default setting).
- 50 µF to 100 µF.

Low Dropout Regulator

Bandwidth of the low dropout regulator has been adapted to improve the load transient response. In case lower ripple is required, internal LDO of the NCV92310 allows using high output capacitor value. In that case, internal stability has to be set thru OTP:

- Up to 50 µF (default setting).
- 50 µF to 100 µF.

STATE MACHINE

The overall operation of the NCV92310 is governed by a state machine that handles the initialization of the IC and the built−in self−test, the fault states, and the different operating modes.

The below diagram represents the behavior as described in the remainder of this document.

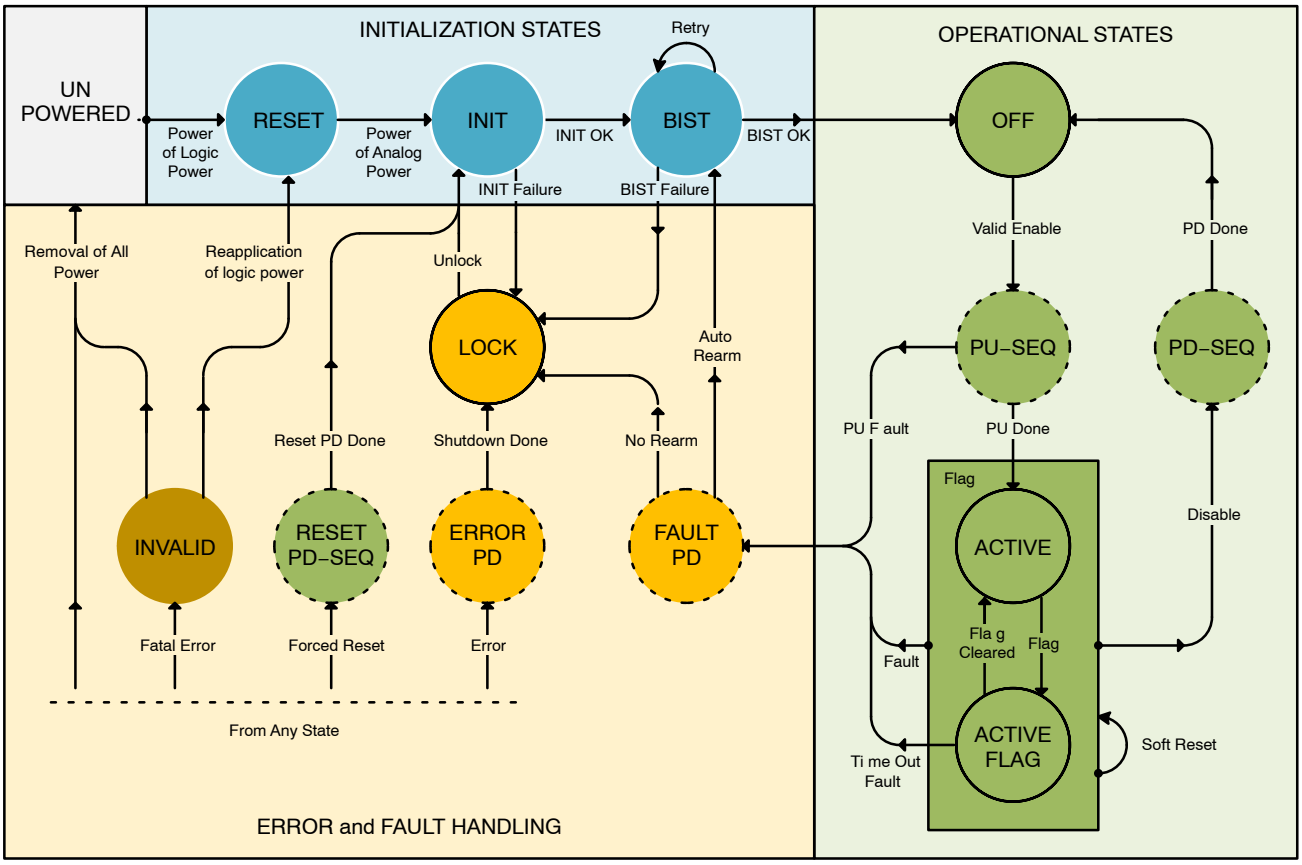

Figure 18. Default State Machine

The state machine is comprised of a number of states of which some are only transitional. The state machine transitions from state to state based on certain specific conditions. Below tables provide a detailed description of each of the states as well as of the transitions.

Table 2. STATE MACHINE STATES

Group	State	Type		RSTB	INTB	I²C	Description
NO POWER	–	–		–	–	–	The supply conditions on PVIN1 and VCORE are too low for the state machine to operate.
INITIALIZATION	RESET	Steady		L	L	No	Only the logic circuitry has sufficient supply and is being held in reset.
	INIT	Transitional		L	L	No	Upon entry, all logic is reset to default and OTP content is loaded. The analog circuitry is enabled.
	BIST	Transitional		L	L	No	Upon entry, a built−in self−test is started
OPERATIONAL	OFF	Steady		L	I	R/W	The IC is biased and ready to accept a power up sequence request
	ACTIVE	Steady		R	I	R/W	A power up sequence has been executed and the IC is operating normally
	ACTIVE FLAG	Transitional		R	L	R/W	Similar to ACTIVE but a flag is raised and upon entry a flag timer starts running
	PU−SEQ	Transitional		See PUS	See PUS	R only	Upon entry, a power up sequence is started.
	PD−SEQ	Transitional		See PDS	See PDS	R only	Upon entry, a power down sequence is started
ERROR & FAULT HANDLING	RESET PD−SEQ	Transitional		L	I	R only	Upon entry, a power down sequence is started
	FAULT PD	Transitional		L	I	R only	Upon entry, all supplies are powered down simultaneously. Internal delay equal to PDS Time Out delay is integrated before going to next state
	ERROR PD	Transitional		L	I	R only	Upon entry, all supplies are powered down simultaneously
	LOCK	Steady		L	I	R/W	The state machine is in the safe state with all supplies disabled.
	INVALID	Steady		L	I	No	Upon entry, an emergency powered down is initiated and product set in reset.

L means Low, R means Released, I reflect the actual state of the Interrupts

Table 3. STATE MACHINE TRANSITIONS

Transition	From	To	Description
Application of Logic Power	NO POWER	RESET	PVIN1 becomes greater than the logic undervoltage detection level
Application of Analog Power	RESET	INIT	PVIN1 becomes greater than the PVIN1 undervoltage lockout detection level
INIT Done	INIT	BIST	The initialization has been finished
BIST OK	BIST	OFF	The built−in self−test was successful
BIST Failure	BIST	LOCK	The built−in self−test failed, and the BIST error counter has reached its limit
Retry	BIST	BIST	The built−in self−test failed, the BIST error counter has not reached its limit, and a new built in self−test is started
Valid Enable	OFF	PU−SEQ	A power up sequence is requested through I^2C
PU Done	PU−SEQ	ACTIVE	The power up sequence has been executed and no faults are detected in the sequencing
PU Fault	PU−SEQ	FAULT PD	A fault is detected during the power up sequence
Flag	ACTIVE	ACTIVE FLAG	An event occurred and is signaled to the host through INTB
Flag Cleared	ACTIVE FLAG	ACTIVE	The signaled event is cleared by the host through I^2C before a time out occurs
Time Out Fault	ACTIVE FLAG	FAULT PD	The signaled event is not cleared in time by the host
Disable	ACTIVE & ACTIVE FLAG	PD−SEQ	A power down sequence is requested through I^2C
PD Done	ACTIVE & ACTIVE FLAG	OFF	The power down sequence has been executed
Reset PD Done	RESET PD−SEQ	INIT	The power down sequence has been executed
Soft Reset	ACTIVE & ACTIVE FLAG	ACTIVE & ACTIVE FLAG	The RSTB pin is temporarily made low by the Watchdog engine, or upon request through I^2C
Fault	ACTIVE & ACTIVE FLAG	FAULT PD	A fault is detected that necessitates a power down
Forced reset	Any State	RESET PD−SEQ	A power down sequence is requested through I^2C.
Error	Any State	ERROR PD	An abnormal operation condition has occurred which necessitates a power down
Fatal Error	Any State	INVALID	A short circuit condition is detected at VCORE or an internal clock error occurs
Removal of Logic Power	Any State	UNPOWERED	PVIN1 falls below the logic POR threshold
	INVALID	UNPOWERED	PVIN1 falls below the logic POR threshold. Power cycling is the only way to recover from an internal clock error
Reapplication of Logic Power	INVALID	RESET	VCORE supply recovers its default voltage from a previous short circuit condition
Shutdown Done	ERROR PD	LOCK	The shutdown has been executed
Auto Rearm	FAULT PD	BIST	A shutdown has been executed and the fault counter has not reached its limit. Only allowed if the source of the fault has disappeared.
No Rearm	FAULT PD	LOCK	A shutdown has been executed and the fault counter has reached its limit
Unlock	LOCK	INIT	An unlock has been requested through I^2C or a restart after TSD or UVLO was permitted. The transition is only permitted if the source of the error has disappeared. NOTE: The IC can also be unlocked by cycling power (from any state, removal of logic power and reapplication).

Auto Rearm Description

After a "FAULT", if AutoRearmCnt < AutoRearmCntMax (I^2C and OTP programmable) NCV92310 restart automatically and goes to the BIST state.

if AutoRearmCnt = AutoRearmCntMax, NCV92310 goes in LOCK mode. P_{VIN1} has to be removed and applied again to restart the NCV92310. Otherwise a new power−up sequence is started.

See "INTERRUPTION" and "FUNCTIONAL SAFETY" sections to have the FAULT description.

Table 4. AUTO REARM COUNTER

Bits	AutoRearmCnt_max
00	No restart
01	3
10	15
11	63

Bist Retry Description

BIST error has its own error counter. If BistCnt < BistCnt max, a BIST retry is performed. If BistCnt = BistCntMax (I^2C and OTP programmable), NCV92310 goes in lock mode.

Table 5. BIST COUNTER

Bits	BistCnt_max
0	No retry
1	1

Unlock Description

Once in lock state, NCV92310 regulators are off with INTB and RSTB pins low. Any I^2C command to start a new power−up sequence or enable one of the regulators will be acknowledged, but power up sequence cannot start if the NCV92310 is locked.

To recover, the NCV92310 must receive one of the following unlock commands.

- Cycling power on PVIN1 pin or
- Set high NLOCK bit or
- In case of TSD having TSD_REARM bit set high or
- In case of UVLO having UVLO_REARM bit set high.

After an unlock command, NCV92310 goes in INIT state and reloads the default value of the OTP by resetting all the registers with the exception of the INTERRUPT_FLAG_ERR1 and INTERRUPT_FLAG_ERR2 registers.

Power Up Sequence

All supply rails can be assigned to the power up sequencer. The sequence can be started upon application of power at PVIN1 or through I^2C. The sequence is preprogrammed through OTP but can be overwritten through I^2C as well. Once a sequence is started it cannot be interrupted with the exception of the occurrence of a fault or error.

A sequence is built up out of three portions: initialization, the sequence with its slots, and a sequence done wait period. During the initialization it is verified that all assigned rails have no residual voltage on their outputs. A delay can be inserted before starting the first rail, allowing for a delay between the request for a power up sequence and the actual start. The sequence itself consists of slots, and at each slot, one or more power rails can be enabled. A slot is started after the rails of the previous slot are successfully powered up plus an optional delay. The sequence done wait period is added at the end of the sequence and can be used to delay the RSTB signal.

During the initialization phase, the active discharge on the assigned rails is enabled. If, at the end of the initialization phase, one of the assigned supply rails still has a residual voltage on its output, this event is logged and a power up sequence is not started.

A supply is considered enabled when its output voltage is established above the undervoltage detection thresholds of that rail, including its debounce "See VOLTAGE MONITORING" section.

Each rail needs to power up within a timeout period. In case of a timeout, the sequence is considered fault and a shutdown is engaged. The event, and the rail causing this are logged. The device will attempt a new startup sequence if the conditions allow.

Rails can be enabled while operating the device. When enabling, and if that rail is originally assigned to a power up sequence, it is being verified that the rail powers up within the timeout period. Any violation is logged. The violation can be cleared through I^2C.

The sequence will power up each voltage rail at its default output voltage setting as set through OTP. This default setting can be overwritten through I^2C.

During the power up sequence, and despite the soft start mechanisms in place, it may be that, during the soft start of DCDC1, the PVIN1 trips the undervoltage lockout detection due to an excessive impedance of the coaxial cable. If DCDC1 is assigned to slot 0 and enabled, and only in this specific case, the device enters a hiccup mode. The power up sequence is aborted so the input supply can recover, and once recovered, the device will continue to soft start DCDC1 repeatedly until the rail is successfully powered up within the timeout period. In all other configurations (DCDC1 assigned to another slot, disabled or another rail assigned to slot 0), this recovery procedure is not supported.

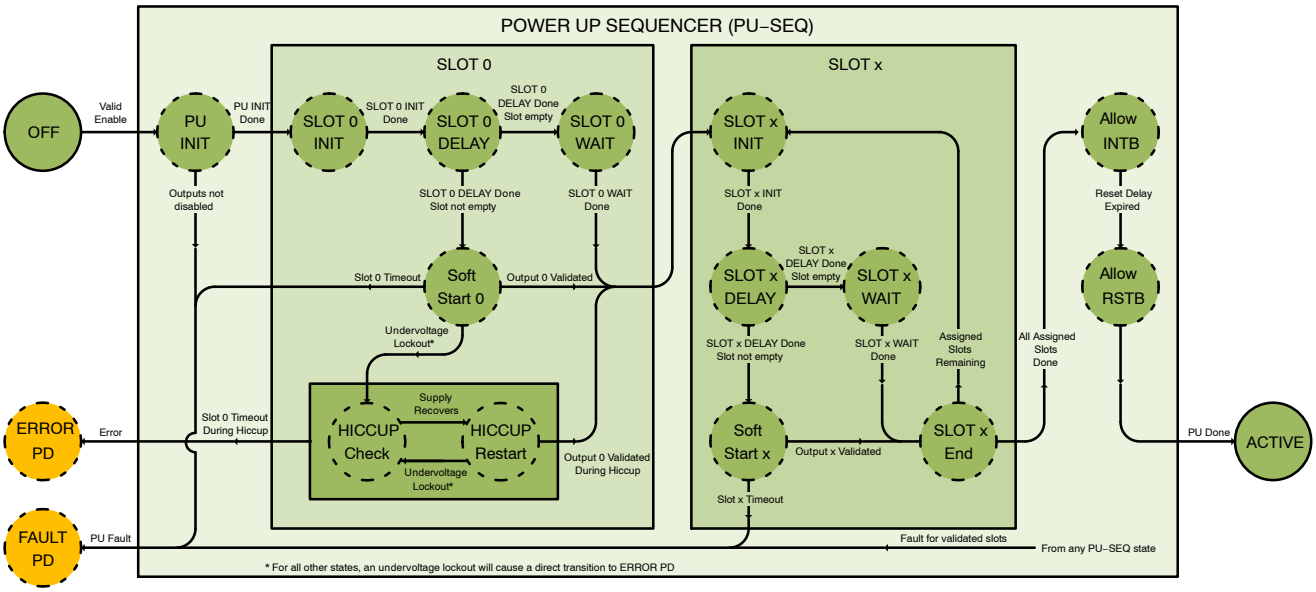

Figure 19. Power−up Sequence State Machine

Table 6. POWER UP SEQUENCER STATES

Group	State	Type	I²C	Description
	PU INIT	Transitional	R only	Only the active discharge on all assigned rails are activated, a timeout is started (64 ms max), the output voltage of the rails are verified with respect to the disable threshold. The state of INTB is frozen and will not change during the power up sequence itself, RSTB is forced low,
	Allow INTB	Transitional	R only	The INTB pin is no longer frozen and reflects the actual state of the interrupts, a sequence done wait timer is started
	Allow RSTB	Transitional	R only	The RSTB pin is released
SLOT 0	SLOT 0 INIT	Transitional	R only	Upon entry, the slot counter is set to 0, the active discharge of the rails assigned to slot 0 are disabled
	SLOT 0 DELAY	Transitional	R only	An initial delay timer is started upon entry
	SLOT 0 WAIT	Transitional	R only	An optional slot length wait timer is started upon entry
	Soft Start 0	Transitional	R only	The slot length timer is started upon entry and the assigned rails are ramped up
	HICCUP Check	Transitional	R only	The ramp up of the assigned rails is stopped, the active discharge remains disabled, the slot length timer continues running, the under voltage lockout is checked.
	HICCUP Restart	Transitional	R only	The soft start resumes. The active discharge remains disabled, the slot length timer continues running.
SLOT x	SLOT x INIT	Transitional	R only	Upon entry the slot counter is increased with +1, the active discharge of the rails assigned to slot x are disabled
	SLOT x DELAY	Transitional	R only	An optional initial delay timer is started upon entry
	SLOT x WAIT	Transitional	R only	An optional slot length wait timer is started upon entry
	Soft Start x	Transitional	R only	The slot length timer is started upon entry and the assigned rails are ramped up
	SLOT x End	Transitional	R only	Upon entry it is verified if there is still an assigned rail on the remaining slots

Table 7. POWER UP SEQUENCER TRANSITIONS

Transition	From	To	Description
Valid Enable	OFF	(PU−SEQ) PU INIT	A power up sequence is requested through I^2C, or, in case the GPIO is configured for this, through the HWEN signal going high.
PU Fault	(PU−SEQ)	FAULT PD	A fault is detected during the power up sequence
Outputs Not Disabled	PU INIT	FAULT PD	After the initialization timeout, one or more of the assigned rails still has a residual voltage above the disable threshold. The state of non−assigned rails has no influence.
PU INIT Done	PU INIT	SLOT 0 INIT	The PU INIT has been executed and no faults are detected
SLOT 0 INIT Done	SLOT 0 INIT	SLOT 0 DELAY	The SLOT 0 INIT has been executed
SLOT 0 DELAY Done, Slot Empty	SLOT 0 DELAY	SLOT 0 WAIT	The initial delay timer has expired and slot 0 is not assigned
SLOT 0 WAIT Done	SLOT 0 WAIT	SLOT x INIT	The optional slot wait timer has expired
SLOT 0 DELAY Done, Slot Not Empty	SLOT 0 DELAY	Soft Start 0	The initial delay timer has expired and slot 0 is assigned
Output 0 Validated	Soft Start 0	SLOT x INIT	The output voltage of all the rails assigned to slot 0 have raised to above the undervoltage detection level for that rail
Slot 0 Timeout	Soft Start 0	FAULT PD	The output voltage of one or more of the rails assigned to slot 0 did not cross the undervoltage detection level for that rail within the slot timeout
Undervoltage Lockout	Soft Start 0 & HICCUP Restart	HICCUP Check	An undervoltage lockout is detected at PVIN1 during the ramp up of DCDC1. This transition is allowed if, and only if, DCDC1 is enabled and assigned to Slot 0. In all other cases an undervoltage lockout is treated as an abnormal operating condition leading to ERROR PD.
Supply Recovers	HICCUP Check	HICCUP Restart	The input supply at PVIN1 raised to above the undervoltage lockout threshold
Output 0 Validated During Hiccup	HICCUP Restart	SLOT x INIT	The output voltage of all the rails assigned to slot 0 have raised to above the undervoltage detection level for that rail
Slot 0 Timeout During Hiccup	HICCUP Check & HICCUP Restart	ERROR PD	The input supply at PVIN1 did not raise to above the undervoltage lockout threshold before the slot timeout, or the rails assigned to slot 0 did not cross the undervoltage detection level for that rail within the slot timeout
SLOT x INIT Done	SLOT x INIT	SLOT x DELAY	The SLOT x INIT has been executed
SLOT x DELAY Done, Slot Empty	SLOT x DELAY	SLOT x WAIT	The initial delay timer has expired and slot x is not assigned
SLOT x WAIT Done	SLOT x WAIT	SLOT x END	The optional slot wait timer has expired
SLOT x DELAY Done, Slot Not Empty	SLOT x DELAY	Soft Start x	The initial delay timer has expired and slot x is assigned
Output x Validated	Soft Start x	SLOT x END	The output voltage of all the rails assigned to slot x have raised to above the undervoltage detection level for that rail
Slot x Timeout	Soft Start x	FAULT PD	The output voltage of one or more of the rails assigned to slot x did not cross the undervoltage detection level for that rail within the slot timeout
Assigned Slots Remaining	SLOT x END	SLOT x INIT	Not all rails that were assigned to the power up sequencer are yet enabled
All Assigned Slots Done	SLOT x END	Allow INTB	All rails that were assigned to the power up sequencer are enabled, the remaining slots will be skipped.
Reset Delay Expired	Allow INTB	Allow RSTB & PG	The sequence done wait timer has expired
PU Done	(PU−SEQ)	ACTIVE	The power up sequence has been executed and no faults are detected in the sequencing
Fault for Validated Slots	Any PU−SEQ State	FAULT PD	A fault has occurred on an already validated slot such as an unexpected undervoltage detection

Power Down Sequence

All supply rails can be assigned to the power down sequencer. The sequence can be started through I^2C. The sequence is preprogrammed through OTP but can be overwritten through I^2C as well. Once a sequence is started it cannot be interrupted.

A sequence is built up out of two portions: an initial delay and the sequence with its slots. The initial delay allows for inserting a delay between the request for a power down sequence and the actual start. The sequence itself consists of slots, and at each slot, one or more power rails can be disabled. A slot is started after the rails of the previous slot are successfully powered down. The INTB and RSTB signal are made low after the initial delay timing.

A supply is considered disabled when its output voltage has fallen below the disable threshold of that rail, "See VOLTAGE MONITORING" section.

Each rail needs to power down within a timeout period. In case of a timeout, this violation is logged but no further specific action is taken. Upon the next power up, the sequence will not be started until all rails that are assigned to the power up sequence are below the disable threshold.

The programming of the power down sequence is fully independent from the power up sequence.

The power down sequence flow diagram and detailed description of each state and transition are provided below.

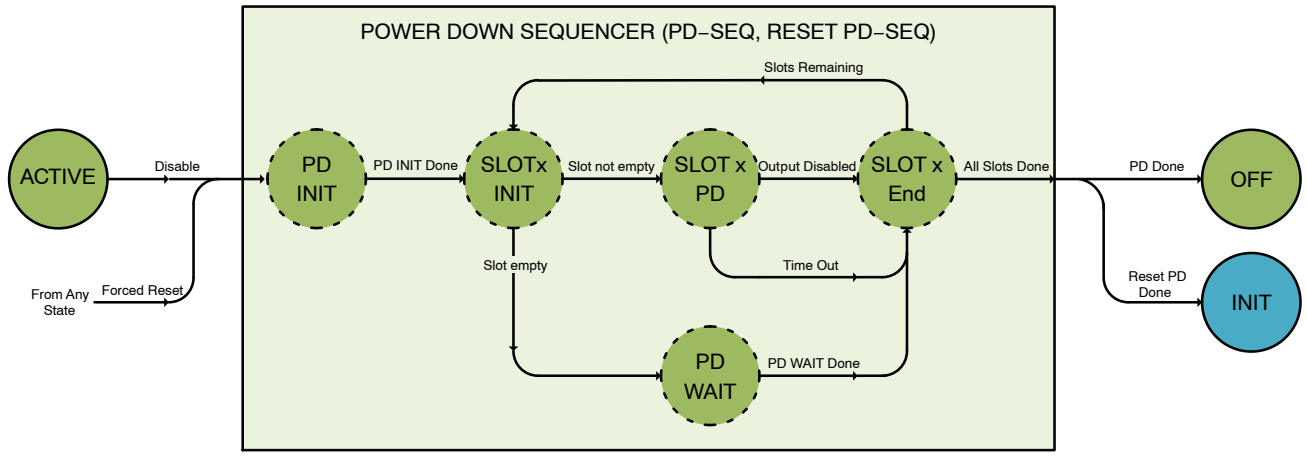

Figure 20. Power Down Sequence State Machine

Table 8. POWER UP SEQUENCER STATES

Group	State	Type	I^2C	Description
Global	PD INIT	Transitional	R only	Upon entry an optional initial delay timer is started
	SLOT x INIT	Transitional	R only	It is verified if slot x has a rail assigned to it
	PD WAIT	Transitional	R only	Upon entry a timeslot wait timer is started
	SLOT x PD	Transitional	R only	For the rails assigned to slot x, the active output discharge is enabled and the output voltage ramped down
	SLOT x End	Transitional	R only	It is verified if there are still slots left to be treated. The slot number is increased by +1

Table 9. POWER UP SEQUENCER TRANSITIONS

Transition	From	To	Description
Disable	ACTIVE	(PD−SEQ) PD INIT	A power down sequence is requested through I^2C.
Forced Reset	Any State	(PD−SEQ) PD INIT	A power down sequence is requested through I^2C.
PD INIT Done	PD INIT	SLOT x INIT	The initial delay timer has expired
Slot Empty	SLOT x INIT	PD WAIT	Slot x has no rail assigned to it
PD WAIT Done	PD WAIT	SLOT x End	The timeslot timer has expired
Slot Not Empty	SLOT x INIT	SLOT x PD	Slot x has one or more rails assigned to it
Output Disabled	SLOT x PD	SLOT x End	The output voltages of all rails assigned to slot x have crossed the disable threshold
Time Out	SLOT x PD	SLOT x End	One or more of the output voltages of the rails assigned to slot x did not cross the disable threshold before the timeslot timer expired
Slots Remaining	SLOT x End	SLOT x INIT	Not all slots have yet been treated (being assigned or not).
All Slots Done, PD Done	(PD−SEQ) SLOT x End	OFF	All slots have been treated and the power down sequence has been executed
All Slots Done, Reset PD Done	(PD−SEQ) SLOT x End	INIT	All slots have been treated and the power down sequence has been executed

INTERRUPTION

In order to inform the system about essential events an interrupt pin INTB is provided. This avoids continuous software pulling for status verification and reduces overall latency for reporting events. There are different interrupt behavior configurations possible.

- Dual edge interrupt: INTB is by default released (high), and is pulled low upon the occurrence of a fault condition or upon the resolution of it. The pin is released when the flag is cleared, even if a fault condition is still present.
- Single edge interrupt: INTB is by default released (high), and is pulled low upon the occurrence of a fault condition. The pin is released when the flag is cleared, even if a fault condition is still present. For INTB released, it is not pulled low upon the resolution of a fault.

Nearly all events have three bits associated: a sense bit, an interrupt flag bit and a mask bit. Below diagrams show the basic functioning of these for all four interrupt configurations. The arrow indicates the edge of the event that influences the other signals.

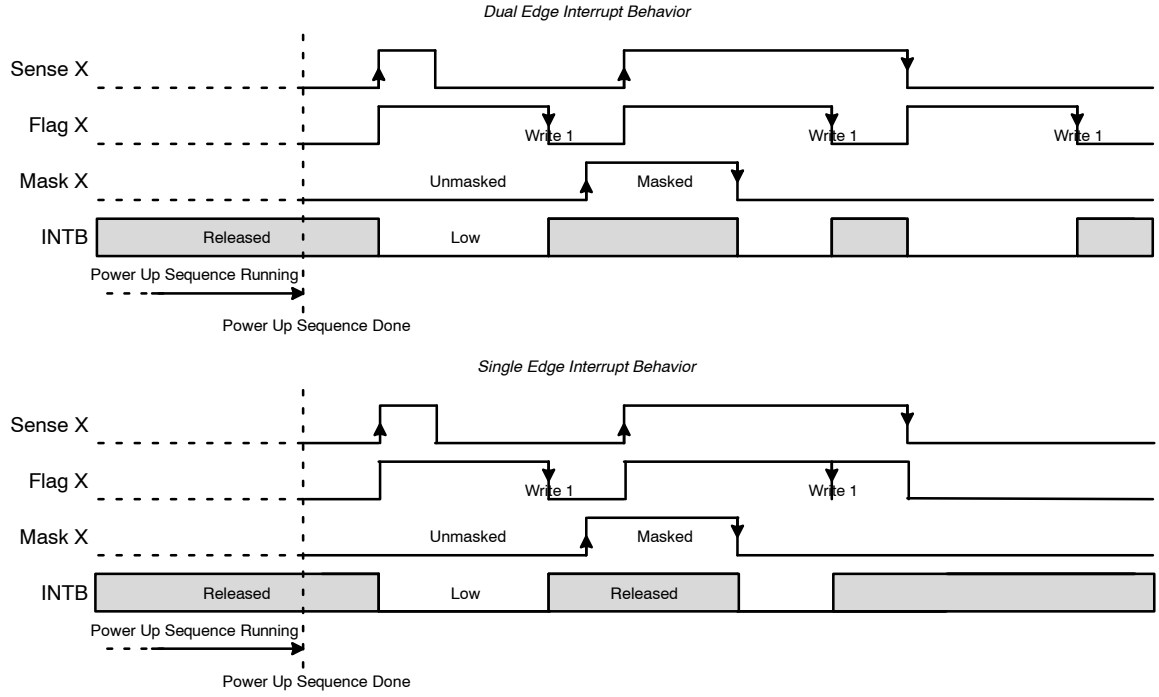

Figure 21. Interrupt Behavior

Below, the behavior of the dual edge interrupt is described, followed by a short description of the differences with the other configurations.

The sense bit reflects the real time status of a detector, like for instance the undervoltage detection of LDO2. When the sense bit changes, the associated interrupt flag bit will be set and latched to a 1. When an interrupt flag bit is 1, the pin INTB is pulled low. An interrupt flag bit is cleared by writing a 1 to the interrupt bit location. If all unmasked interrupt flag bits are cleared the INTB pin will be released. The INTB line will only go high if no other device on the bus continuous to pull it low.

Each interrupt flag bit has an associated mask bit. When the mask bit is set 1 the interrupt flag bit value is of no influence on the interrupt pin INTB. Masking interrupt bits will make sure only the most essential interrupts will cause INTB to be pulled low. Mask bit default settings depends on OTP configuration.

Given the number of possible interrupts and in order to reduce the read−out time, a status register regroups all

interrupts of the same type to a single bit. Only unmasked interrupts will be reflected through the status bits. As an example, if one of the unmasked undervoltage interrupts is generated, the undervoltage status bit is also set. By reading only the status register software can decide if the type of interrupt is of high importance or verify that the IC is the one that pulled the interrupt line low.

In case of a single edge interrupt configuration, the behavior of the sense bits is identical to that of the dual edge configuration. The behavior of the interrupt flag bit and INTB behavior is slightly different. Like for the dual edge interrupt, when the sense bit changes from 0 to a 1, the associated interrupt flag bit will be set and latched to a 1. This interrupt flag bit can be cleared by writing a 1 which will release the INTB pin, however, as long as the corresponding sense bit remains high, the read back of the

flag bit stays a 1. A cleared flag bit will automatically read back a 0 when the corresponding sense bit reverts to 0. This way, the INTB pin will only be forced low upon the detection of the event reflected by the sense bit, but not when the event disappears. The mask bit behavior is identical to the dual edge configuration.

After the startup of the device the INTB pin (push−pull configuration) is driven low and will be driven high at the end of the power –up sequence. If a flag event has occurred during the power−up sequence, NCV92310 will keep the pin low until the flag is cleared.

Due to defects, such as short to supply, the interrupt line might stay high permanently. Therefore, I^2C content should be consulted after power up even if the interrupt line pin is not going low in order to verify the integrity of the interrupt line. A dedicated read/write bit is provided to force INTB low if set to 1 or let INTB released when set to 0 in order to assist the system in verifying the overall signal integrity.

Table 10. INTERRUPT SOURCES (ERROR)

Interrupt Sources	Description
OVERTEMP (ERROR)	
TSD	Thermal Shutdown
SELF TEST FAILURE (ERROR)	
BIST	BIST error
OTP_ERROR	Error not corrected during OTP loading
ABNORMAL OPERATING CONDITIONS (ERROR)	
SC_DCDC1	Short Circuit DCDC1
SC_DCDC2	Short Circuit DCDC2
SC_DCDC3	Short Circuit DCDC3
SC_LDO1	Short Circuit LDO1
SC_SW1_DCDC1	DCDC1 SW pin
SC_SW2_DCDC2	DCDC2 SW pin
SC_SW3_DCDC3	DCDC3 SW pin
I2C_REGERROR	Register map integrity error
UVLO	UVLO state
OVE	Input Over Voltage Error (input overvoltage flag disable)
FB1 open	DCDC1 feedback pin open
CORE FAILURE (FATAL ERROR)	
SC_VCORE	Short Circuit Internal Vcore Supply
Clock_Error	Internal Clock Error

Table 11. INTERRUPT SOURCES (FAULT AND FLAG)

Interrupt Sources	Description
FAULT	
Fault_Time_Out	Time out when in ACTIVE FLAG mode
PUS_FAIL	Power up sequence Failure
UVT_BUCK1	DCDC1 Under Voltage Threshold
OVT_BUCK1	DCDC1 Over Voltage Threshold
FLAG	
DCDC1_IPK pos	DCDC1 Converter Positive Inductor Peak Current Protection
DCDC1_IPK neg	DCDC1 Converter Negative Inductor Peak Current Protection
DCDC2_IPK pos	DCDC2 Converter Positive Inductor Peak Current Protection
DCDC2_IPK neg	DCDC2 Converter Negative Inductor Peak Current Protection
DCDC3_IPK pos	DCDC3 Converter Positive Inductor Peak Current Protection
DCDC3_IPK neg	DCDC3 Converter Negative Inductor Peak Current Protection
LDO1_OCP	LDO1 Output Over Current
I2C_FAIL	I^2C communication lost
I2C_CRC_ERROR	I^2C communication error
TSD_PWRNG	Thermal Pre−Warning
TSD_WRNG	Thermal Warning
OVF	Input Over Voltage Flag (input overvoltage error disable)
PDS_FAIL	Power down sequence Failure
FAULT OR FLAG (DEPENDS ON OTP CONFIGURATION)	
UVT_BUCK2	DCDC2 Under Voltage Threshold
OVT_BUCK2	DCDC2 Over Voltage Threshold
UVT_BUCK3	DCDC3 Under Voltage Threshold
OVT_BUCK3	DCDC3 Over Voltage Threshold
UVT_LDO1	LDO1 Under Voltage Threshold
OVT_LDO1	LDO1 Over Voltage Threshold
FB2_OPEN	DCDC2 feedback pin open
FB3_OPEN	DCDC3 feedback pin open

FUNCTIONAL SAFETY

NCV92310 embeds several safety mechanism, which allow the part to be ASIL B compliant.

Voltage Monitoring

NCV92310 integrates four windows voltage monitoring (one per channel). During normal operation, the under voltage comparator is used to detect if an established supply rail does not go below the under voltage threshold V_{UV} while the overvoltage comparator is used to detect if a supply rail does not exceed the overvoltage threshold V_{OV}.

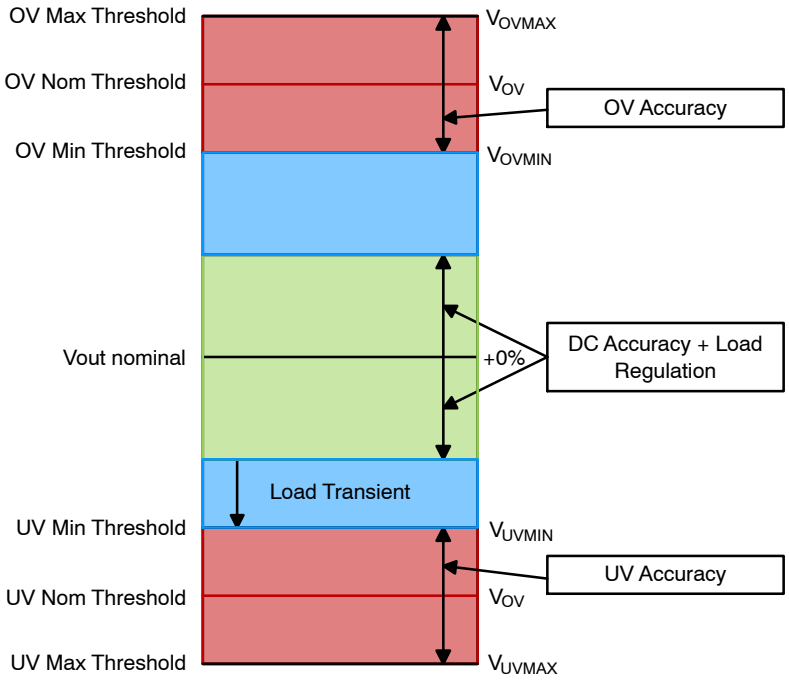

Figure 22.

Overall monitoring accuracy is the sum of multiple accuracies:

- DC Accuracy.
- Load and Line Regulation.
- OV or OV monitoring accuracy.
- Load transient.

DC Accuracy, Load Regulation, Line Regulation, OV monitoring accuracy and UV monitoring accuracy are specified in the parametric table (see Electrical Characteristics section).

Load transient performance is dependent on both the NCV92310 and application implementation. The NCV92310 internal regulators load transient performance depends on the $\Delta I / \Delta t$ and C_{OUT}. It can be estimated with the following equation:

$$\Delta V = \frac{\Delta I}{2 \times \pi \times \text{COUT derated} \times \text{BW}} \quad \text{(eq. 3)}$$

V_{UVMAX} and V_{OVMAX} are the maximum value of the monitoring threshold. V_{UV} and V_{OV} are I^2C and OTP programmable with the following nominal thresholds:

A second bandgap is dedicated to the voltage monitoring to reach high level of functional safety.

NCV92310 windows monitoring function embeds digital filters which validate that the output of the comparators do not change state during the programmed debounce time. For each given channel, the debounce time T_{L_F} for the undervoltage falling edge, the T_{L_R} for the rising edge, as well as the T_{H_R} for the overvoltage rising edge and T_{H_F} for the falling edge are all independently programmable. The debouncers are programmable in a ratiometric fashion. This means that every next binary code will multiply the debounce of the previous binary code by a factor of 2, see parametric table for more details.

The digital filters can be bypassed for the undervoltage falling edge TL_F and the overvoltage rising edge TH_R. In that case the comparator output gets latched to avoid any synchronization error with the clock digital circuitry.

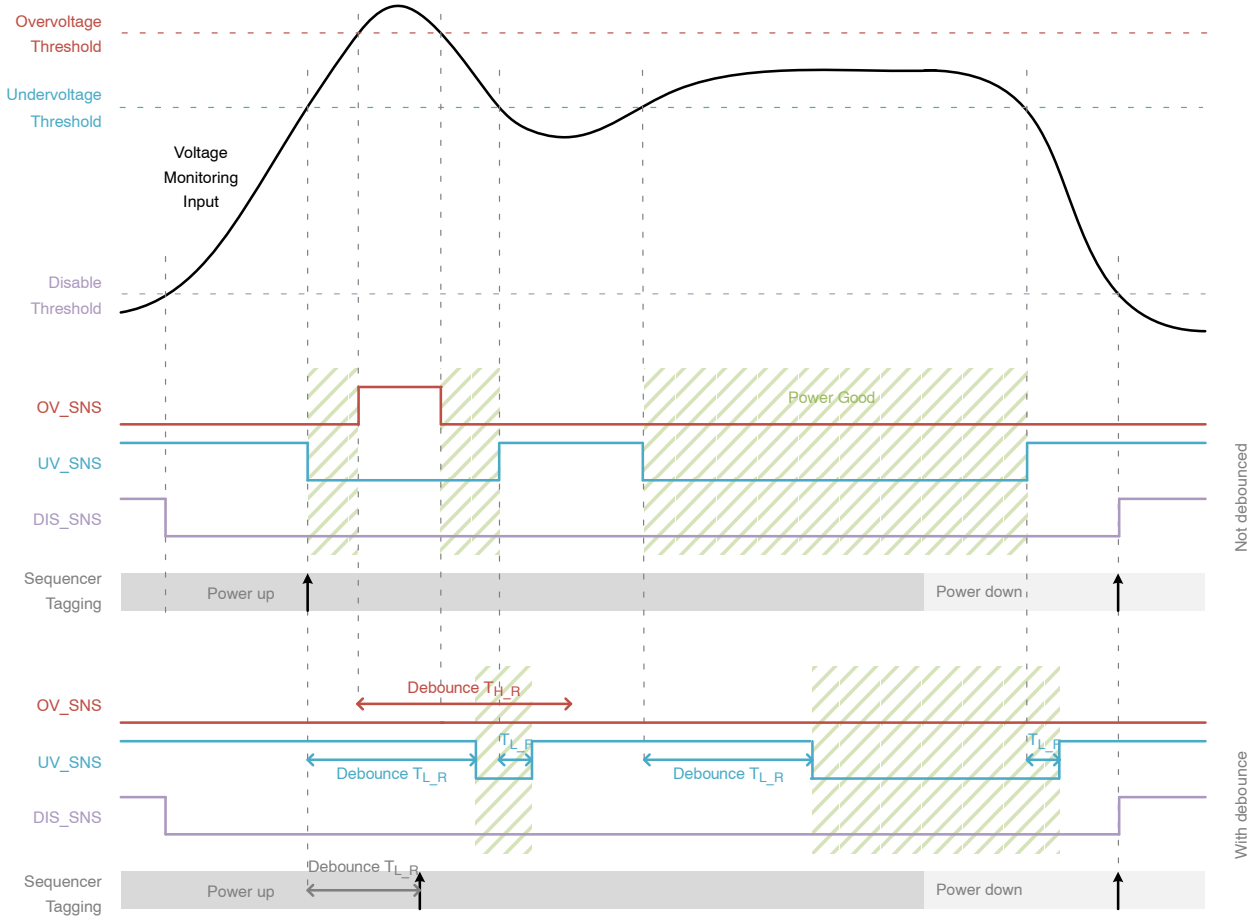

Figure 23. Illustration of Comparator Behavior

Output voltages of DCDC1, DCDC2, DCDC3, LDO1 shall be at their respective VOUT targets with a tolerance window defined by VH and VL.

Any violation of the respective VOUT windows greater than their respective TH_R or TL_F debounce time shall be detected.

Once one of the output voltages cross a V_{OV} or V_{UV} threshold, /INT goes low and in respect with the OTP/I^2C configuration DCDCs and LDO are turned off and /RST pin goes low.

VCORE Short Circuit Protection

Once a short circuit protection is detected in the VCORE pin, the NCV92310 goes into the RESET state until the short is removed. Short circuit current is limited at ≈ 60 mA.

Clock Error Protection

NCV92310 embeds a 2 MHz system clock in addition of the 2.15 MHz DCDCs clock.

Once one regulator is turned on, availability and shift of the 2 MHz clock is monitored. In case of failure, NCV92310 is locked in RESET state. To recover, PVIN1 has to be removed and re−applied again.

Self Test

- *ECC*

  A One Time Programmable memory with Error Code Correction is embedded with 6 ECC bits and 26 OTP bits per 32 OTP bits bank.

  If one error is detected per bank, internal ECC correct the failing bit and ACK_BIST bit is flagged.

  If 2 errors are detected per bank, part goes in lock mode and ACK_BIST bit is flagged. To recover, ACK_BIST bit has to be cleared and an unlock command has to be done: set high the NLOCK bit or remove and re−apply PVIN.

- *Windows voltage monitoring self test*

  At startup, an internal self test validate the windows voltage monitoring functionality (BIST state in the STATE MACHINE) :

  - Overvoltage and undervoltage detection.
  - Overvoltage and undervoltage hysteresis functionality.
  - Leakage detection.
  - Offset calibration.

  If failed ACK_BIST is set high. One retry can be done if BistCnt bit is set high (OTP and I^2C configurable). Otherwise part goes in lock mode.

I²C Register Map Integrity Checking

Integrity of the configuration register in the register map is monitored continuously. If one configuration bit changed without the appropriate I²C command, NCV92310 goes in LOCK state.

I²C Communication Lost Protection

To be able to check that the I²C communication operates properly and allow the system to do the appropriate action once a fault is flagged thru the interrupt pin, system has to write periodically in the I2CTMOUT register with a period defined by the I2C_TIMEOUT bits in the IC_CONFIGURATION_I2CTMOUT register.

If not done, NCV92310 will flag the system thru the interrupt pin, which goes in ACTIVE Flag state and flag the dedicated acknowledge bit.

DCDC Positive Current Limitation

The internal DCDCs protect the device from over current with a fixed−value cycle−by−cycle current limitation. If inductor current exceeds the current limit threshold, the High Side Switch will be turned off cycle−by−cycle. Due to the propagation delay of the internal comparator, dynamic current limitation can be higher than the peak current threshold that is set internally.

The maximum peak current in the inductor can be computed with:

$$I_{PEAKPOS} = I_{LIMP} + \frac{(V_{IN} - V_{OUT})}{L} \times T_{DELAY} \quad \text{(eq. 4)}$$

With $T_{DELAY\ DCDC1}$ = 30 ns (typ) and $T_{DELAY\ DCDC2/DCDC3}$ = 40 ns (typ).

The maximum output current can be computed with:

$$I_{MAX} = I_{PEAK} + \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{2 \times V_{IN} \times f_{SW} \times L} \quad \text{(eq. 5)}$$

Where V_{IN} is input supply voltage, V_{OUT} is output voltage, L is inductance of the filter inductor, and F_{SW} is 2.15 MHz normal switching frequency.

DCDC Negative Current Protection

In addition, to protect the Low Side switch, the negative current protection (Ipeakn) limits potential excessive current from output (for example, when fault condition causes the output voltage to be higher than the nominal output voltage).

The maximum negative peak current in the inductor can be computed with:

$$I_{PEAKNEG} = -I_{LIMN} - \frac{V_{OUT}}{L} \times T_{DELAY} \quad \text{(eq. 6)}$$

With $T_{DELAY\ DCDC1}$ = 50 ns (typ) and $T_{DELAY\ DCDC2/DCDC3}$ = 20 ns (typ).

DCDC Short Circuit Protection

To protect against excessive load or short circuit to ground, if 2 Ipeak pos are counted when in power fail (so when V_{UV} is trigged) the NCV92310 goes in ERROR PD state with all the rail turned off immediately.

To protect against excessive short to high voltage, if 2 Ipeak neg are counted when in power fail (so when V_{OV} is trigged) the NCV92310 goes in ERROR PD state with all the rail turned off immediately.

DCDC Switching Node Short Circuit Protection

NCV92310 embeds a short circuit on the SW pin of each regulator to avoid any damage in the part due to excessive current thru the internal output power stage. Once a short circuit is detected, part is turned OFF.

DCDC1 embeds a protection from SW1 to PGND1. DCDC2 and DCDC3 embeds a protection from SW2/3 to PVIN2/3 and PGND2/3.

Protection in case of internal short between PVIN1 and SW1. IC will flag it but it will not remove the short and avoid any damage thru the inductor on FB1 and PVIN2/PViN3/VINLDO if these 3 pins are connected at the output of the DCDC1.

DCDCs Feedback Pin Open Protection

DCDC1

FB1 pin is connected internally to a resistor bridge. In case of open, internally the input of the error amplifier will be tied to ground and undervoltage detection will be triggued and NCV92310 turned off.

DCDC2 and DCDC3

FB2 and FB3 pins, in addition of the connection to the error amplifier, are tied to Vin internally. Output voltage will decrease and overvoltage detection will be triggued to avoid any damage to the IC which are supplied by the NCV92310.

LDO Over Current Protection and Output Short Circuit Protection

The low drop out regulator (LDO) on the IC is based on an embedded PMOS and requires no external stability components or feedback networks.

The output must be bypassed with at least a 2.2 μF ceramic capacitor.

Internal LDO includes an over current protection circuit ($I_{LIMITLDO}$). Once crossed, the dedicated acknowledge bit is set high to advise the system that the LDO is overloaded.

After crossing the $I_{LIMITLDO}$, if the load continue to increase internal LDO will start to deregulate. A short circuit protection is embedded with I_{SCLDO} set 15 mA higher than $I_{LIMITLDO}$. Once in short circuit, NCV92310 goes in ERROR PD state and all the regulators are turned off immediately.

Under Voltage Lockout

The input voltage PVIN1 must reach or exceed the UVLO rising threshold before the NCV92310 enables the converter output to begin the power up sequence.

When PVIN1 cross the UVLO falling threshold, no power down sequence is expected. All the supplies are disabled and output discharged simultaneously.

UVLO Thresholds and hysteresis are I²C and OTP programmable to fit multiple camera applications use cases.

Over Voltage Detection

To protect from input voltage higher than 18V, NCV92310 includes an internal comparator in the PVIN1 pin. Depending on the OTP configuration:

- NCV92310 will flag the system thru the /INT pin if a supply voltage higher than 18.3 V (typical) is detected on PVIN1 input. System has to safely turn off the load of the NCV92310 before removing the power supply if the OverVoltage is still present. Otherwise the system has to clear the fault in the dedicated acknowledge bit.
- NCV92310 will turn off all the regulators, pull low INTB and RSTB pins and goes in lock state.

Thermal Protection

NCV92310 has a thermal shutdown protection to protect the device from overheating. After the thermal protection is triggered, All the supplies are disabled and output discharged simultaneously.

NCV92310 includes a thermal warning and thermal pre−warning thresholds to advise the system that the die temperature has become too high. The dedicated ACK_THERMAL_PRWNG, ACK_THERMAL_WNG bits and /INT pin are flagged depending on the MSK_THERMAL_PRWNG and MSK_THERMAL_WNG setting. Thermal Warning Threshold is the last flag before going in TSD and shutdown the part.

Thermal Pre−Warning threshold is I^2C and OTP programmable.

If TSD_REARM bit is high, NCV92310 recovers automatically and goes to the INIT state to reload the OTP and restart with the default settings.

To prevent the camera application, and in particular the image sensor, from powering up under too high ambient temperature conditions, the power up sequence is conditioned by the die temperature of the IC. Before engaging a power up sequence, the on−chip dissipation is close to zero, which makes that the die temperature of the IC will be a good representation of the ambient temperature. (Thermal gating threshold, can be deactivated by I^2C / OTP).

Fault Time Out

Once in Active Flag state after an internal FLAG highlighted to the system thru the /INT pin, system has to clear the dedicated acknowledge bit within a delay set thru the FAULT_TIMEOUT[0:1] bits. If not done, NCV92310 goes in FAULT PD state and can restart or goes in lock mode depending on the AutoRearm setting. ACK_FAULT_TIMEOUT bit is set high to highlight the fault.

Power−up Sequence Fail

During the PUS, if a rail does not reach its default value by triggering its undervoltage rising monitoring threshold once the SLOT time out is done, NCV92310 goes in FAULT PD state and flag the ACK_PUS bit.

Power−down Sequence Fail

During the PDS, if a rail does not reach the $V_{DISABLE}$ threshold once the SLOT time out is done, NCV92310 continue the power down sequence but flag the ACK_PUS bit and /INT pin goes low.

I²C COMPATIBLE INTERFACE

NCV92310 can support a subset of the I²C protocol as detailed below (Read, Write, Write then read sequences).

I2C Communication Description

The device is widely programmable through an I²C compatible interface available at SCL and SDA. The I²C interface has no dedicated I/O supply and the logic low and high levels are therefore fixed and not adjusted to the actual drive levels. Events are signaled on a side signal at INTB. The address of the device on the I²C bus is 7−bit long of which the 3 bits can be set with OTP.

For robust I²C transfers an 8−bit CRC (cyclic redundancy check) mechanism is implemented with fixed CRC code X8+X2+X+1. This is the same code as used in SMBus communication, for more information refer to the System Management Bus Specification version 3.1, sections 6.4 and 6.5 (specifically, refer to section 6.4.1.3 for details on slave implementation). The CRC−coding can be enabled or disabled based on OTP setting and I²C programming.

With CRC−coding disabled, single byte write and read as well as continuous write and read are supported. With CRC−coding enabled, only single byte write and read are supported. In the latter case an 8−bit PEC (packet error code) is transmitted as the last byte of the transfer. Below, the protocol is shown in detail for the different use cases, with and without CRC.

When using CRC, for a write access, the PEC is calculated over the 3 bytes included in the entire transfer from Start to Stop. This includes the I²C address and R/W bit, the register address and the data, but excludes the (Repeated)Start/Stop and the ACK/NACK signaling. The PEC is appended by the master as the second data byte at the end of the transfer. If the PEC received by the slave does not correspond the PEC byte calculated by the slave, the data written will be ignored and the transaction will be NACKed by the slave. Since also the NACK could get corrupted an interrupt is generated as well.

For a read access the PEC is calculated over the 4 bytes included in the entire transfer from Start to Stop. This includes the I²C address and R/W bit, the register address, again the I²C address and R/W bit and the data, but excludes the (Repeated) Start/Stop and the ACK/NACK signaling. The PEC is appended by the slave as the second data byte at the end of the transfer.

For clarification, the bytes over which the PEC is calculated are highlighted in below diagram.

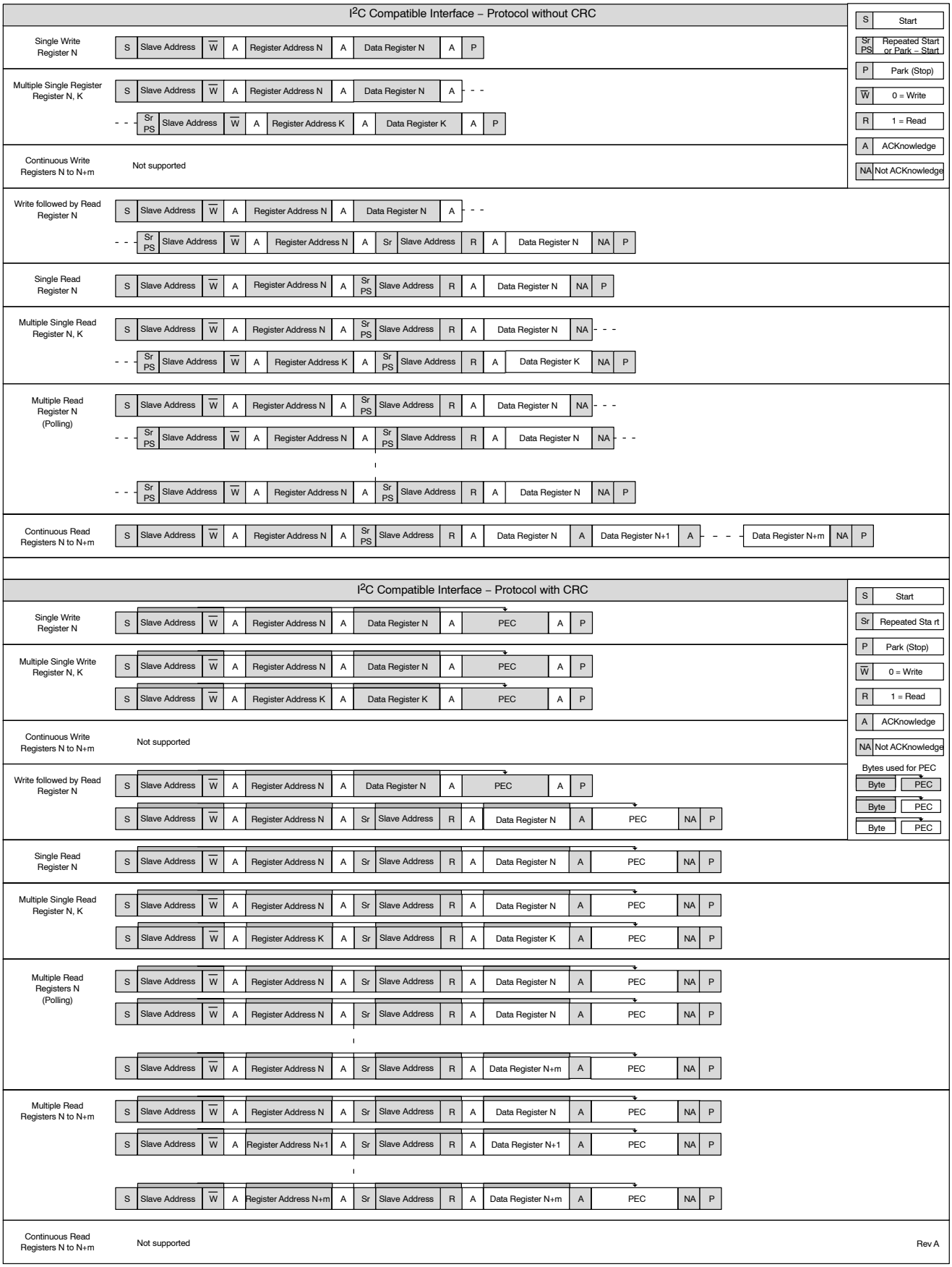

Figure 24. I²C Bus Protocol

I²C Slave Address

The NCV92310 has 8 available I²C addresses selectable by factory settings (ADD0 to ADD7). Different address settings can be generated upon request to **onsemi**.

Table 12. I²C SLAVE ADDRESS

I²C Slave Address	Hex	A7	A6	A5	A4	A3	A2	A1	A0
ADD0	W 0x20 R 0x21	0	0	1	0	0	0	0	R/W
	Add								–
ADD1 (default)	W 0x28 R 0x29	0	0	1	0	1	0	0	R/W
	Add								–
ADD2	W 0x30 R 0x31	0	0	1	1	0	0	0	R/W
	Add								–
ADD3	W 0x38 R 0x39	0	0	1	1	1	0	0	R/W
	Add								–
ADD4	W 0xC0 R 0xC1	1	1	0	0	0	0	0	R/W
	Add								–
ADD5	W 0xC8 R 0xC9	1	1	0	0	1	0	0	R/W
	Add								–
ADD6	W 0xD0 R 0xD1	1	1	0	1	0	0	0	R/W
	Add								–
ADD7	W 0xD8 R 0xD9	1	1	0	1	1	0	0	R/W
	Add								–

I²C UNLOCK Write Protected Register

By default, all the registers after the UNLOCK_WRITE_PROTECT_REG register are locked. Only read access is allowed.

To write in a register, user has to send a write command with 0x69 in the unlock register, and then send a write command with the register address to write. Once the write command has been sent to the unlocked register with the write data, this register is locked again.

Table 13. REGMAP

Addr	Register Name	Register Type	Def.	Function
0h	PID	R	00111010b (3Ah)	Product Id
1h	RID	R	00000000b (0h)	Revision Id
2h	FID	R	00000000b (0h)	Features Id
3h	INT_STATUS	R	00000000b (0h)	Interrupt Status Register
4h	INTERRUPT_FLAG_IC	W1CSingle	00000000b (0h)	Interrupt Flag IC Acknowledge Register
5h	INTERRUPT_FLAG_ERR1	W1CSingle	00000000b (0h)	Interrupt Flag Error Acknowledge Register 1
6h	INTERRUPT_FLAG_ERR2	W1CSingle	00000000b (0h)	Interrupt Flag Error Acknowledge Register 2
7h	INTERRUPT_FLAG_OV	W1CSingle	00000000b (0h)	Interrupt Flag Over Voltage Threshold Monitoring Acknowledge Register
8h	INTERRUPT_FLAG_UV	W1CSingle	00000000b (0h)	Interrupt Flag Under Voltage Threshold Monitoring Acknowledge Register
9h	INTERRUPT_FLAG_OC	W1CSingle	00000000b (0h)	Interrupt Over Current Acknowledge Register
0Ah	INTERRUPT_SENSE_IC	R	00000000b (0h)	Interrupt Flag IC Sense Register
0Bh	INTERRUPT_SENSE_ERR	R	00000000b (0h)	Interrupt Flag Error System Sense Register
0Ch	INTERRUPT_SENSE_OV	R	00000000b (0h)	Interrupt Flag Over Voltage Threshold Monitoring Sense Register
0Dh	INTERRUPT_SENSE_UV	R	00000000b (0h)	Interrupt Flag Under Voltage Threshold Monitoring Sense Register
0Eh	IC_STATUS_DISCHARGED	R	00000000b (0h)	IC output discharged status register
0Fh	IC_STATUS_SAFE_STATE	R	00000000b (0h)	IC Regulator safe state status register
10h	IC_STATUS_MISCELLANEOUS_1	R	00000000b (0h)	IC status error counter register
11h	IC_STATUS_MISCELLANEOUS_2	R	00000000b (0h)	IC status state machine counter register
12h	I2CTMOUT	RW	00000000b (0h)	I^2C Timeout Write register
13h	UNLOCK_WRITE_PROTECT_REG	RW	00000000b (0h)	Unlock Register
14h	IC_CONFIGURATION_I2CTMOUT	CRC	00000000b (0h)	I^2C timeout setting register
15h	IC_CONFIGURATION_1	CRC	00100101b (25h)	IC Configurations Register 1
16h	IC_CONFIGURATION_2	CRC	00000000b (0h)	IC Configurations Register 2
17h	IC_CONFIGURATION_3	CRC	00001100b (Ch)	IC Configurations Register 3
18h	IC_CONFIGURATION_4	CRC	00000000b (0h)	IC Configurations Register 4
19h	INTERRUPT_MASK_IC	CRC	00000000b (0h)	Interrupt Flag IC Mask Register
1Ah	INTERRUPT_MASK_OV	CRC	00000000b (0h)	Interrupt mask register Overvoltage monitoring threshold
1Bh	INTERRUPT_MASK_UV	CRC	00000000b (0h)	Interrupt mask register Undervoltage monitoring threshold
1Ch	INTERRUPT_MASK_OC	CRC	00101010b (2Ah)	Interrupt mask register Overcurrent protection
1Dh	OUTPUT_VOLTAGE_DCDC1	CRC	00000101b (5h)	DCDC1 Output Voltage Programmation Register
1Eh	CONFIGURATION_DCDC1	CRC	00001101b (Dh)	DCDC1 Configuration register
1Fh	OUTPUT_VOLTAGE_DCDC2	CRC	00011000b (18h)	DCDC2 Output Voltage Programmation Register
20h	CONFIGURATION_DCDC2	CRC	00001101b (Dh)	DCDC2 Configuration register
21h	OUTPUT_VOLTAGE_DCDC3	CRC	00110000b (30h)	DCDC3 Output Voltage Programmation Register
22h	CONFIGURATION_DCDC3	CRC	00001101b (Dh)	DCDC3 Configuration register
23h	OUTPUT_VOLTAGE_LDO1	CRC	00000010b (2h)	LDO1 Output Voltage Programmation Register
24h	CONFIGURATION_LDO1	CRC	00001101b (Dh)	LDO1 Configuration register

Table 13. REGMAP (continued)

Addr	Register Name	Register Type	Def.	Function
25h	MONITORING_UV_DCDC1	CRC	00100100b (24h)	Monitoring Undervoltage DCDC1 settings
26h	MONITORING_OV_DCDC1	CRC	01010000b (50h)	Monitoring Overvoltage DCDC1 settings
27h	MONITORING_UV_DCDC2	CRC	00100100b (24h)	Monitoring Undervoltage DCDC2 settings
28h	MONITORING_OV_DCDC2	CRC	01010000b (50h)	Monitoring Overvoltage DCDC2 settings
29h	MONITORING_UV_DCDC3	CRC	00100100b (24h)	Monitoring Undervoltage DCDC3 settings
2Ah	MONITORING_OV_DCDC3	CRC	01010000b (50h)	Monitoring Overvoltage DCDC3 settings
2Bh	MONITORING_UV_LDO1	CRC	00100100b (24h)	Monitoring Undervoltage LDO1 settings
2Ch	MONITORING_OV_LDO1	CRC	01010000b (50h)	Monitoring Overvoltage LDO1 settings
2Dh	SEQUENCER_ASSIGNMENT_DCDC1	CRC	00000000b (0h)	Sequencer Assignment DCDC1 register
2Eh	SEQUENCER_ASSIGNMENT_DCDC2	CRC	00010001b (11h)	Sequencer Assignment DCDC2 register
30h	SEQUENCER_ASSIGNMENT_DCDC3	CRC	00100010b (22h)	Sequencer Assignment DCDC3 register
31h	SEQUENCER_ASSIGNMENT_LDO1	CRC	00110011b (33h)	Sequencer Assignment LDO1 register
32h	SEQUENCER_CONFIGURATION_1	CRC	00001101b (Dh)	Sequencer configuration register 1
33h	SEQUENCER_CONFIGURATION_2	CRC	01101011b (6Bh)	Sequencer configuration register 2

Table 14. PRODUCT ID

Register Name		PID	**Address**	00
Type		R	**Default**	00111010b (3Ah)
Trigger				
Bit	**Name**	**Description**		
7	PID	Product Id		
6				
5				
4				
3				
2				
1				
0				

Table 15. REVISION ID

Register Name		RID	Address	01
Type		R	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	RID	Revision Id		
6				
5				
4				
3				
2				
1				
0				

Table 16. FEATURES ID

Register Name		FID	Address	02
Type		R	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	FID	Features Id		
6				
5				
4				
3				
2				
1				
0				

Table 17. INTERRUPT STATUS REGISTER

Register Name		INT_STATUS	Address	03
Type		R	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	ST_OC	Status bit Over current Fault Or between FLAG_OC bits (unmasked bits)		
4	ST_DIS	Status bit disable threshold not crossed during a PDS		
3	ST_MUV	Status bit monitoring undervoltage Or between FLAG_OV bits (unmasked bits)		
2	ST_MOV	Status bit monitoring overvoltage Or between FLAG_OV bits (unmasked bits)		
1	ST_ERR	Status bit Interrupt flar error Or between FLAG_ERR bits (unmasked bits)		
0	ST_IC	Status bit flag IC Or between FLAG_IC bits (unmasked bits)		

Table 18. INTERRUPT FLAG IC ACKNOWLEDGE REGISTER

Register Name		INTERRUPT_FLAG_IC	Address	04
Type		W1CSingle	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	ACK_PDS	Power down sequence Fault Acknowledge 0: Cleared 1: Event Detected		
6	ACK_PUS	Power up sequence Fault Acknowledge 0: Cleared 1: Event Detected		
5	ACK_TSD_WRNG	Thermal Warning Fault Acknowledge 0: Cleared 1: Event Detected		
4	ACK_TSD_PTWRNG	Thermal Pre−Warning Fault Acknowledge 0: Cleared 1: Event Detected		
3	ACK_I2CFAIL	Watchdog Fault Acknowledge 0: Cleared 1: Event Detected		
2	ACK_FAULT_TIMEOUT	Fault timeout Acknowledge 0: Cleared 1: Event Detected		
1	ACK_I2CERROR	I^2C interface CRC Fault Acknowledge 0: Cleared 1: Event Detected		
0	ACK_OVF	Input Over Voltage Detection Flag Acknowledge (depends on OTP configuration) 0: Cleared 1: Event Detected		

Table 19. INTERRUPT FLAG ERROR ACKNOWLEDGE REGISTER 1

Register Name		INTERRUPT_FLAG_ERR1	Address	05
Type		W1CSingle	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	ACK_FRCRST	Force reset power down sequence 0: cleared 1: Force Reset done		
6	ACK_UVLO	Input Under Voltage Threshold Fault Acknowledge 0: Cleared 1: Event Detected		
5	ACK_TSD	Thermal Shutdown Fault Acknowledge 0: Cleared 1: Event Detected		
4	empty			
3	ACK_OVE	Input Over Voltage Detection Error Acknowledge (depends on OTP configuration) 0: Cleared 1: Event Detected		
2	ACK_AUTOREARMCNT	Auto Rearm Error Acknowledge 0: Cleared 1: Event Detected		
1	ACK_I2CREGERROR	Write Register CRC Fault Acknowledge 0: Cleared 1: Event Detected		
0	ACK_BIST	BIST Fault Acknowledge (BIST or OTP ECC Error) 0: Cleared 1: Event Detected		

Table 20. INTERRUPT FLAG ERROR ACKNOWLEDGE REGISTER 2

Register Name		INTERRUPT_FLAG_ERR2	Address	06
Type		W1CSingle	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	ACK_SC_SW_DCDC3	DCDC3 Short Circuit Protection 0: Cleared 1: Event Detected		
5	ACK_SC_SW_DCDC2	DCDC2 Short Circuit Protection 0: Cleared 1: Event Detected		
4	ACK_SC_SW_DCDC1	DCDC1 Short Circuit Protection 0: Cleared 1: Event Detected		
3	ACK_SC_LDO1	LDO1 Short Circuit Protection 0: Cleared 1: Event Detected		
2	ACK_SC_VOUT_DCDC3	DCDC3 Short Circuit Protection 0: Cleared 1: Event Detected		
1	ACK_SC_VOUT_DCDC2	DCDC2 Short Circuit Protection 0: Cleared 1: Event Detected		
0	ACK_SC_VOUT_DCDC1	DCDC1 Short Circuit Protection 0: Cleared 1: Event Detected		

Table 21. INTERRUPT FLAG OVER VOLTAGE THRESHOLD MONITORING ACKNOWLEDGE REGISTER

Register Name		INTERRUPT_FLAG_OV	Address	07
Type		W1CSingle	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	ACK_OV_LDO1	LDO1 Monitoring Over Voltage Threshold Acknowledge 0: Cleared 1: Event Detected		
2	ACK_OV_DCDC3	DCDC3 Monitoring Over Voltage Threshold Acknowledge 0: Cleared 1: Event Detected		
1	ACK_OV_DCDC2	DCDC2 Monitoring Over Voltage Threshold Acknowledge 0: Cleared 1: Event Detected		
0	ACK_OV_DCDC1	DCDC1 Monitoring Over Voltage Threshold Acknowledge 0: Cleared 1: Event Detected		

Table 22. INTERRUPT FLAG UNDER VOLTAGE THRESHOLD MONITORING ACKNOWLEDGE REGISTER

Register Name		INTERRUPT_FLAG_UV	Address	08
Type		W1CSingle	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	ACK_UV_LDO1	LDO1 Monitoring Under Voltage Threshold Acknowledge 0: Cleared 1: Event Detected		
2	ACK_UV_DCDC3	DCDC3 Monitoring Under Voltage Threshold Acknowledge 0: Cleared 1: Event Detected		
1	ACK_UV_DCDC2	DCDC2 Monitoring Under Voltage Threshold Acknowledge 0: Cleared 1: Event Detected		
0	ACK_UV_DCDC1	DCDC1 Monitoring Under Voltage Threshold Acknowledge 0: Cleared 1: Event Detected		

Table 23. INTERRUPT OVER CURRENT ACKNOWLEDGE REGISTER

Register Name		INTERRUPT_FLAG_OC	Address	09
Type		W1CSingle	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	ACK_LDO1_OCP	LDO1 Over Current Protection Acknowledge 0: Cleared 1: Event Detected		
5	ACK_IPEAK_NEG_DCDC3	DCDC3 Negative current limitation Acknowledge 0: Cleared 1: Event Detected		
4	ACK_IPEAK_POS_DCDC3	DCDC3 Inductor IPEAK current limitation Acknowledge 0: Cleared 1: Event Detected		
3	ACK_IPEAK_NEG_DCDC2	DCDC2 Negative current limitation Acknowledge 0: Cleared 1: Event Detected		
2	ACK_IPEAK_POS_DCDC2	DCDC2 Inductor IPEAK current limitation Acknowledge 0: Cleared 1: Event Detected		
1	ACK_IPEAK_NEG_DCDC1	DCDC1 Negative current limitation Acknowledge 0: Cleared 1: Event Detected		
0	ACK_IPEAK_POS_DCDC1	DCDC1 Inductor IPEAK current limitation Acknowledge 0: Cleared 1: Event Detected		

Table 24. INTERRUPT FLAG IC SENSE REGISTER

Register Name		INTERRUPT_SENSE_IC	Address	0A
Type		R	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	SEN_TSD_WRNG	TSD Warning Sense 0: Thermal warning below threshold 1: Thermal warning above threshold		
4	SEN_TSD_PRWRNG	TSD Pre−Warning Sense 0: Thermal Pre−warning below threshold 1: Thermal Pre−warning above threshold		
3	empty			
2	empty			
1	empty			
0	SEN_OVF	OVF Sense 0: PVIN1 below threshold 1: PVIN1 above threshold		

Table 25. INTERRUPT FLAG ERROR SYSTEM SENSE REGISTER

Register Name		INTERRUPT_SENSE_ERR	Address	0B
Type		R	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	SEN_UVLO	UVLO Sense 0: PVIN1 above threshold 1: PVIN1 below threshold		
5	SEN_TSD	TSD Sense 0: Thermal Shutdown below threshold 1: Thermal shutdown above threshold		
4	empty			
3	empty			
2	empty			
1	empty			
0	empty			

Table 26. INTERRUPT FLAG OVER VOLTAGE THRESHOLD MONITORING SENSE REGISTER

Register Name		INTERRUPT_SENSE_OV	Address	0C
Type		R	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	SEN_OV_LDO1	LDO1 Monitoring Over Voltage Threshold Sense 0: LDO1 Output Voltage within nominal range 1: LDO1 Output Voltage Above Target		
2	SEN_OV_DCDC3	DCDC3 Monitoring Over Voltage Threshold Sense 0: DCDC3 Output Voltage within nominal range 1: DCDC3 Output Voltage Above Target		
1	SEN_OV_DCDC2	DCDC2 Monitoring Over Voltage Threshold Sense 0: DCDC2 Output Voltage within nominal range 1: DCDC2 Output Voltage Above Target		
0	SEN_OV_DCDC1	DCDC1 Monitoring Over Voltage Threshold Sense 0: DCDC1 Output Voltage within nominal range 1: DCDC1 Output Voltage Above Target		

Table 27. INTERRUPT FLAG UNDER VOLTAGE THRESHOLD MONITORING SENSE REGISTER

Register Name		INTERRUPT_SENSE_UV	Address	0D
Type		R	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	SEN_UV_LDO1	LDO1 Monitoring Over Voltage Threshold Sense 0: LDO1 Output Voltage within nominal range 1: LDO1 Output Voltage Above Target		
2	SEN_UV_DCDC3	DCDC3 Monitoring Over Voltage Threshold Sense 0: DCDC3 Output Voltage within nominal range 1: DCDC3 Output Voltage Above Target		
1	SEN_UV_DCDC2	DCDC2 Monitoring Over Voltage Threshold Sense 0: DCDC2 Output Voltage within nominal range 1: DCDC2 Output Voltage Above Target		
0	SEN_UV_DCDC1	DCDC1 Monitoring Over Voltage Threshold Sense 0: DCDC1 Output Voltage within nominal range 1: DCDC1 Output Voltage Above Target		

Table 28. IC OUTPUT DISCHARGED STATUS REGISTER

Register Name		IC_STATUS_DISCHARGED	Address	0E
Type		R	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	*OVLO_SAFE*	OVLO SafeState status 0: DCDC1 windows monitoring used a interrupt 1: DCDC1 windows monitoring used as Error (safetstate)		
3	S_LDO1_DIS	Status bit for LDO1 discharge during previous PD SEQ		
2	S_DCDC3_DIS	Status bit for DCDC3 discharge during previous PD SEQ		
1	S_DCDC2_DIS	Status bit for DCDC2 discharge during previous PD SEQ		
0	S_DCDC1_DIS	Status bit for DCDC1 discharge during previous PD SEQ		

Table 29. IC REGULATOR SAFE STATE STATUS REGISTER

Register Name		IC_STATUS_SAFE_STATE	Address	0F
Type		R	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	*LDO1_OV_SAFE*	LDO1 SafeState status 0: LDO1 windows monitoring used a interrupt 1: LDO1 windows monitoring used as Error (safetstate)		
6	*DCDC3_OV_SAFE*	DCDC3 SafeState status 0: DCDC3 windows monitoring used a interrupt 1: DCDC3 windows monitoring used as Error (safetstate)		
5	*DCDC2_OV_SAFE*	DCDC2 SafeState status 0: DCDC2 windows monitoring used a interrupt 1: DCDC2 windows monitoring used as Error (safetstate)		
4	*DCDC1_OV_SAFE*	DCDC1 SafeState status 0: DCDC1 windows monitoring used a interrupt 1: DCDC1 windows monitoring used as Error (safetstate)		
3	*LDO1_UV_SAFE*	LDO1 SafeState status 0: LDO1 windows monitoring used a interrupt 1: LDO1 windows monitoring used as Error (safetstate)		
2	*DCDC3_UV_SAFE*	DCDC3 SafeState status 0: DCDC3 windows monitoring used a interrupt 1: DCDC3 windows monitoring used as Error (safetstate)		
1	*DCDC2_UV_SAFE*	DCDC2 SafeState status 0: DCDC2 windows monitoring used a interrupt 1: DCDC2 windows monitoring used as Error (safetstate)		
0	*DCDC1_UV_SAFE*	DCDC1 SafeState status 0: DCDC1 windows monitoring used a interrupt 1: DCDC1 windows monitoring used as Error (safetstate)		

Table 30. IC STATUS ERROR COUNTER REGISTER

Register Name		IC_STATUS_MISCELLANEOUS_1	Address	10
Type		R	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	STAT_BIST	Bist done		
6	AutoRearmCnt_STAT	Auto Rearm Counter status. Counter resetted when AutoRearmCnt_RST bit is set to 1		
5				
4				
3				
2				
1				
0				

Table 31. IC STATUS STATE MACHINE COUNTER REGISTER

Register Name		IC_STATUS_MISCELLANEOUS_2	Address	11
Type		R	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	STATPU	00: PUS ok 01: Rail required discharged 10: Restart required due to UVLO for DCDC1 in SLOT0 11: Rail required discharged and Restart required due to UVLO for DCDC1 in SLOT0		
6				
5	STATSLOTPU	00: No slot timeout fault 100: Slot timeout SLOT 0 101: Slot timeout SLOT 1 110: Slot timeout SLOT 2 111: Slot timeout SLOT 3 (updated at the end of the PUS)		
4				
3				
2	STATMCH	State Machine status 000: OFF 001: PU−SEQ 010: ACTIVE − ACTIVE FLAG 011: PD−SEQ 100: FAULT PD 101: ERROR PD 110: RESET−SEQ 111: LOCK		
1				
0				

Table 32. I²C TIMEOUT WRITE REGISTER

Register Name		I2CTMOUT	Address	12
Type		RW	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	empty			
2	empty			
1	empty			
0	I2C_TIMEOUT_WR	I²C access to this register has to be done continuously with a max period defined by the I²C Time Out delay. If not done, the dedicated ACK bit is flagged and /INT pin is pulled low.		

Table 33. UNLOCK REGISTER

Register Name		UNLOCK_WRITE_PROTECT_REG	Address	13
Type		RW	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	UNLOCK	8 bits to unlock configuration registers. By default, configuration registers are locked to avoid unexpected change thru I^2C		
6				
5				
4				
3				
2				
1				
0				

Table 34. I^2C TIMEOUT SETTING REGISTER

Register Name		IC_CONFIGURATION_I2CTMOUT	Address	14
Type		CRC	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	empty			
2	empty			
1	*I2C_TIMEOUT*	2 bits for I^2C communication timeout 00: disable 01: 16 ms 10: 128 ms 11: 1024 ms		
0				

Table 35. IC CONFIGURATIONS REGISTER 1

Register Name		IC_CONFIGURATION_1	Address	15
Type		CRC	Default	00100101b (25h)
Trigger				
Bit	**Name**	**Description**		
7	UVLO_REARM	UVLO Auto rearm when in lock mode: 0: no rearm. 1: auto rearm.		
6	TSD_REARM	TSD Auto rearm when in lock mode: 0: no rearm. 1: auto rearm.		
5	TSD_Gating	Avoid startup of power−up sequence if Tj > 125°C 0: disable 1: enable		
4	TSD_PRWRNG	Thermal shutdown pre−warning selection 0: 140°C 1: 130°C		
3 2 1 0	UVLO	UVLO Programmability: Rising Falling 0000: 4.5 V 4.3 V 0001: 6.0 V 4.3 V 0010: 7.0 V 4.3 V 0011: 8.0 V 4.3 V 0100: 6.0 V 5.0 V 0101: 7.0 V 5.0 V 0110: 8.0 V 5.0 V 0111: 6.0 V 5.5 V 1000: 7.0 V 5.5 V 1001: 8.0 V 5.5 V 1010: 7.0 V 6.0 V 1011: 8.0 V 6.0 V 1100: N/A N/A 1101: N/A N/A 1110: N/A N/A 1111: N/A N/A		

Table 36. IC CONFIGURATIONS REGISTER 2

Register Name		IC_CONFIGURATION_2	Address	16
Type		CRC	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	*CRCEN*	I^2C communication CRC enable 0: I^2C communication without CRC 1: I^2C communication with CRC		
5	AutoRearmCnt_RST	Once set to 1, internal error counter is resetted. This bit is self cleared to 0 once the counter is resetted.		
4	empty			
3 2	*AutoRearmCnt*	Safe state auto restart: 00: No restart 01: 3 restarts 10: 15 restarts 11: 63 restarts		
1	empty			
0	*BistCnt*	BIST Retry: 0: no retry 1: one retry		

Table 37. IC CONFIGURATIONS REGISTER 3

Register Name		IC_CONFIGURATION_3	Address	17
Type		CRC	Default	00001100b (Ch)
Trigger				
Bit	**Name**	**Description**		
7	FRCINTB	Bit to force interrupt pin low or high 0: INTB follow the state machine description 1: INTB pin forced low		
6	NLOCK	NLOCK bit when NCV92310 in lock mode. Self cleared once done. 0: no unlock 1: NCV92310 unlocked		
5	*FAULT_TIMEOUT*	2 bits for Active Flag Mode state timeout: 00: disable 01: 45 ms 10: 95 ms 11: 150 ms		
4				
3	*Soft_RST_Timer*	Soft Reset Timer: 00: 1 ms 01: 4 ms 01: 16 ms 11: 64 ms		
2				
1	Soft_RST	Soft Reset bit: 0: no soft reset. 1: /RST pin pulled low. Timing set in the Soft Reset Timer. Self cleared once done		
0	Forced_RST	Forced Reset bit: 0: no reset 1: Reset, NCV92310 will start a Power down sequence followed by a BIST and a Power up Sequence. Bit is cleared once done.		

Table 38. IC CONFIGURATIONS REGISTER 4

Register Name		IC_CONFIGURATION_4	Address	18
Type		CRC	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	*SPREAD_FSW*	Spread Spectrum Switching Frequency Variation: 0: 10% max 1: 5% max		
3	*SPREAD_MODF*	Spread spectrum divider (frequency changed every x cycles) LFSR Triangular 00: Divider = 1, Divider = 4 01: Divider = 2, Divider = 5 10: Divider = 3, Divider = 6 11: Divider = 4, Divider = 7		
2				
1	*SPREAD_MODT*	Spread Spectrum modulation scheme 0: LFSR (16 bits Pseudo random equal distribution) 1: Triangular (dual peak)		
0	*SPREAD_EN*	Spread Spectrum Enable bit: 0: Disable 1: Enable		

Table 39. INTERRUPT FLAG IC MASK REGISTER

Register Name		INTERRUPT_MASK_IC	Address	19
Type		CRC	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	MSK_TSD_WRNG	Thermal Shutdown Warning Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked		
4	MSK_TSD_PRWRNG	Thermal Shutdown Pre−Warning Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked		
3	empty			
2	empty			
1	MSK_I2CERROR	I^2C communication error Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked OTP bit available to desactivate the whole function		
0	MSK_OVF	OVD Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked OTP bit available to desactivate the whole function		

Table 40. INTERRUPT MASK REGISTER OVERVOLTAGE MONITORING THRESHOLD

Register Name		INTERRUPT_MASK_OV	Address	1A
Type		CRC	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	MSK_OV_LDO1	LDO1 Monitoring Over Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked If LDO1_SAFE bit is set high, fault cannot be masked		
2	MSK_OV_DCDC3	DCDC3 Monitoring Over Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked If DCDC3_SAFE bit is set high, fault cannot be masked		
1	MSK_OV_DCDC2	DCDC2 Monitoring Over Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked If DCDC2_SAFE bit is set high, fault cannot be masked		
0	MSK_OV_DCDC1	DCDC1 Monitoring Over Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked If DCDC1_SAFE bit is set high, fault cannot be masked		

Table 41. INTERRUPT MASK REGISTER UNDERVOLTAGE MONITORING THRESHOLD

Register Name		INTERRUPT_MASK_UV	Address	1B
Type		CRC	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	MSK_UV_LDO1	LDO1 Monitoring Under Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked If LDO1_SAFE bit is set high, fault cannot be masked		
2	MSK_UV_DCDC3	DCDC3 Monitoring Under Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked If DCDC3_SAFE bit is set high, fault cannot be masked		
1	MSK_UV_DCDC2	DCDC2 Monitoring Under Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked If DCDC2_SAFE bit is set high, fault cannot be masked		
0	MSK_UV_DCDC1	DCDC1 Monitoring Under Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked If DCDC1_SAFE bit is set high, fault cannot be masked		

Table 42. INTERRUPT MASK REGISTER OVERCURRENT PROTECTION

Register Name		INTERRUPT_MASK_OC	Address	1C
Type		CRC	Default	00101010b (2Ah)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	MSK_LDO1_OCP	LDO1 Over Current Protection Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked		
5	*MSK_IPEAK_NEG_DCDC3*	DCDC3 Negative current limitation Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked OTP bit available to mask the /INTB pin pulled low when Ipeak neg is triggered		
4	MSK_IPEAK_POS_DCDC3	DCDC3 Inductor IPEAK current limitation Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked		
3	*MSK_IPEAK_NEG_DCDC2*	DCDC2 Negative current limitation Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked OTP bit available to mask the /INTB pin pulled low when Ipeak neg is triggered		
2	MSK_IPEAK_POS_DCDC2	DCDC2 Inductor IPEAK current limitation Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked		
1	*MSK_IPEAK_NEG_DCDC1*	DCDC1 Negative current limitation Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked OTP bit available to mask the /INTB pin pulled low when Ipeak neg is triggered		
0	MSK_IPEAK_POS_DCDC1	DCDC1 Inductor IPEAK current limitation Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked		

Table 43. DCDC1 OUTPUT VOLTAGE PROGRAMMATION REGISTER

Register Name		OUTPUT_VOLTAGE_DCDC1	Address	1D
Type		CRC	Default	00000101b (5h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	*VDCDC1*	DCDC1 Output Voltage Programmability 0000: 2.8 V 0001: 2.9 V 0010: 3.0 V 0011: 3.1 V 0100: 3.2 V 0101: 3.3 V 0110: 3.4 V 0111: 3.5 V 1000: 3.6 V 1001: 3.8 V 1010: 4.0 V 1011: 4.2 V 1100: 4.4 V 1101: 4.6 V 1101: 4.8 V 1111: 5.0 V		
0				

Table 44. DCDC1 CONFIGURATION REGISTER

Register Name		CONFIGURATION_DCDC1	Address	1E
Type		CRC	Default	00001101b (Dh)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	DIS_DCDC1	DCDC1 active output discharge 0: Disabled (valid if PWR SEQ_EN = 0) 1: Enabled		
2	*Soft_Start_DCDC1*	2 bits to set the DCDC1 soft start 00: 0.08 ms/V 01: 0.16 ms/V 10: 0.32 ms/V 11: 0.64 ms/V		
1				
0	*ENDCDC1*	DCDC1 enable bit: (valid if SEQ_EN = 0) 0: Disabled 1: Enabled		

Table 45. DCDC2 OUTPUT VOLTAGE PROGRAMMATION REGISTER

Register Name		OUTPUT_VOLTAGE_DCDC2	Address	1F
Type		CRC	Default	00011000b (18h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	*VDCDC2*	DCDC2 Output Voltage Programmability From 0.6 V to 2.175 V with 25 mV Step		
4				
3				
2				
1				
0				

Table 46. DCDC2 CONFIGURATION REGISTER

Register Name		CONFIGURATION_DCDC2	Address	20
Type		CRC	Default	00001101b (Dh)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	DIS_DCDC2	DCDC2 active output discharge 0: Disabled (valid if PWR SEQ_EN = 0) 1: Enabled		
2	*Soft_Start_DCDC2*	2 bits to set the DCDC2 soft start 00: 0.08 ms/V 01: 0.16 ms/V 10: 0.32 ms/V 11: 0.64 ms/V		
1				
0	*ENDCDC2*	DCDC2 enable bit: (valid if SEQ_EN = 0) 0: Disabled 1: Enabled		

Table 47. DCDC3 OUTPUT VOLTAGE PROGRAMMATION REGISTER

Register Name		OUTPUT_VOLTAGE_DCDC3	Address	21
Type		CRC	Default	00110000b (30h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	*VDCDC3*	DCDC3 Output Voltage Programmability From 0.6 V to 2.175 V with 25 mV Step		
4				
3				
2				
1				
0				

Table 48. DCDC3 CONFIGURATION REGISTER

Register Name		CONFIGURATION_DCDC3	Address	22
Type		CRC	Default	00001101b (Dh)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	DIS_DCDC3	DCDC3 active output discharge 0: Disabled (valid if PWR SEQ_EN = 0) 1: Enabled		
2	*Soft_Start_DCDC3*	2 bits to set the DCDC3 soft start 00: 0.08 ms/V 01: 0.16 ms/V 10: 0.32 ms/V 11: 0.64 ms/V		
1				
0	*ENDCDC3*	DCDC3 enable bit: (valid if SEQ_EN = 0) 0: Disabled 1: Enabled		

Table 49. LDO1 OUTPUT VOLTAGE PROGRAMMATION REGISTER

Register Name		OUTPUT_VOLTAGE_LDO1	Address	23
Type		CRC	Default	00000010b (2h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	empty			
2	*VLDO1*	LDO1 Output Voltage Programmability From 2.6 V to 3.3 V with 100 mV step		
1				
0				

Table 50. LDO1 CONFIGURATION REGISTER

Register Name		CONFIGURATION_LDO1	Address	24
Type		CRC	Default	00001101b (Dh)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	empty			
4	empty			
3	DIS_LDO1	LDO1 active output discharge 0: Disabled (valid if PWR SEQ_EN = 0) 1: Enabled		
2 1	*Soft_Start_LDO1*	2 bits to set the LDO1 soft start 00: 0.16 ms/V 01: 0.32 ms/V 10: 0.64 ms/V 11: 1.28 ms/V		
0	*ENLDO1*	LDO1 enable bit: (valid if SEQ_EN = 0) 0: Disabled 1: Enabled		

Table 51. MONITORING UNDERVOLTAGE DCDC1 SETTINGS

Register Name		MONITORING_UV_DCDC1	Address	25
Type		CRC	Default	00100100b (24h)
Trigger				
Bit	**Name**	**Description**		
7 6 5	*DCDC1_UVT*	DCDC1 Under Voltage Monitoring Threshold in % of the programmed output voltage: 000: −3.0% 001: −3.5% 010: −4.0% 011: −4.5% 100: −5.0% 101: −6.0% 110: −8.0% 111: −10%		
4 3	*DCDC1_DBN_TLR*	Debounce Rising edge programmability: 00: 32 μs 01: 64 μs 10: 128 μs 11: 256 μs		
2 1 0	*DCDC1_DBN_TLF*	Debounce falling edge programmability: 000: none 001: 2 μs 010: 4 μs 011: 8 μs 100: 16 μs 101: 32 μs 110: 64 μs 111: 128 μs		

Table 52. MONITORING OVERVOLTAGE DCDC1 SETTINGS

Register Name		MONITORING_OV_DCDC1	Address	26
Type		CRC	Default	01010000b (50h)
Trigger				
Bit	**Name**	**Description**		
7	*DCDC1_OVT*	DCDC1 Under Voltage Monitoring Threshold in % of the programmed output voltage: 000: 3.0% 001: 3.5% 010: 4.0% 011: 4.5% 100: 5.0% 101: 6.0% 110: 8.0% 111: 10%		
6				
5				
4	*DCDC1_DBN_THR*	Debounce rising edge programmability: 000: none 001: 2 μs 010: 4 μs 011: 8 μs 100: 16 μs 101: 32 μs 110: 64 μs 111: 128 μs		
3				
2				
1	*DCDC1_DBN_THF*	Debounce falling edge programmability: 00: 32 μs 01: 64 μs 10: 128 μs 11: 256 μs		
0				

Table 53. MONITORING UNDERVOLTAGE DCDC2 SETTINGS

Register Name		MONITORING_UV_DCDC2	Address	27
Type		CRC	Default	00100100b (24h)
Trigger				
Bit	**Name**	**Description**		
7	*DCDC2_UVT*	DCDC2 Under Voltage Monitoring Threshold in % of the programmed output voltage: 000: −3.0% 001: −3.5% 010: −4.0% 011: −4.5% 100: −5.0% 101: −6.0% 110: −8.0% 111: −10%		
6				
5				
4	*DCDC2_DBN_TLR*	Debounce Rising edge programmability: 00: 32 μs 01: 64 μs 10: 128 μs 11: 256 μs		
3				
2	*DCDC2_DBN_TLF*	Debounce falling edge programmability: 000: none 001: 2 μs 010: 4 μs 011: 8 μs 100: 16 μs 101: 32 μs 110: 64 μs 111: 128 μs		
1				
0				

Table 54. MONITORING OVERVOLTAGE DCDC2 SETTINGS

Register Name		MONITORING_OV_DCDC2	Address	28
Type		CRC	Default	01010000b (50h)
Trigger				
Bit	**Name**	**Description**		
7	*DCDC2_OVT*	DCDC2 Under Voltage Monitoring Threshold in % of the programmed output voltage: 000: 3.0% 001: 3.5% 010: 4.0% 011: 4.5% 100: 5.0% 101: 6.0% 110: 8.0% 111: 10%		
6				
5				
4	*DCDC2_DBN_THR*	Debounce rising edge programmability: 000: none 001: 2 μs 010: 4 μs 011: 8 μs 100: 16 μs 101: 32 μs 110: 64 μs 111: 128 μs		
3				
2				
1	*DCDC2_DBN_THF*	Debounce falling edge programmability: 00: 32 μs 01: 64 μs 10: 128 μs 11: 256 μs		
0				

Table 55. MONITORING UNDERVOLTAGE DCDC3 SETTINGS

Register Name		MONITORING_UV_DCDC3	Address	29
Type		CRC	Default	00100100b (24h)
Trigger				
Bit	**Name**	**Description**		
7	*DCDC3_UVT*	DCDC3 Under Voltage Monitoring Threshold in % of the programmed output voltage : 000: −3.0% 001: −3.5% 010: −4.0% 011: −4.5% 100: −5.0% 101: −6.0% 110: −8.0% 111: −10%		
6				
5				
4	*DCDC3_DBN_TLR*	Debounce Rising edge programmability: 00: 32 μs 01: 64 μs 10: 128 μs 11: 256 μs		
3				
2	*DCDC3_DBN_TLF*	Debounce falling edge programmability: 000: none 001: 2 μs 010: 4 μs 011: 8 μs 100: 16 μs 101: 32 μs 110: 64 μs 111: 128 μs		
1				
0				

Table 56. MONITORING OVERVOLTAGE DCDC3 SETTINGS

Register Name		MONITORING_OV_DCDC3	Address	2A
Type		CRC	Default	01010000b (50h)
Trigger				
Bit	**Name**	**Description**		
7	*DCDC3_OVT*	DCDC3 Under Voltage Monitoring Threshold in % of the programmed output voltage: 000: 3.0% 001: 3.5% 010: 4.0% 011: 4.5% 100: 5.0% 101: 6.0% 110: 8.0% 111: 10%		
6				
5				
4	*DCDC3_DBN_THR*	Debounce rising edge programmability: 000: none 001: 2 μs 010: 4 μs 011: 8 μs 100: 16 μs 101: 32 μs 110: 64 μs 111: 128 μs		
3				
2				
1	*DCDC3_DBN_THF*	Debounce falling edge programmability: 00: 32 μs 01: 64 μs 10: 128 μs 11: 256 μs		
0				

Table 57. MONITORING UNDERVOLTAGE LDO1 SETTINGS

Register Name		MONITORING_UV_LDO1	Address	2B
Type		CRC	Default	00100100b (24h)
Trigger				
Bit	**Name**	**Description**		
7	*LDO1_UVT*	LDO1 Under Voltage Monitoring Threshold in % of the programmed output voltage : 000: −3.0% 001: −3.5% 010: −4.0% 011: −4.5% 100: −5.0% 101: −6.0% 110: −8.0% 111: −10%		
6				
5				
4	*LDO1_DBN_TLR*	Debounce Rising edge programmability: 00: 32 μs 01: 64 μs 10: 128 μs 11: 256 μs		
3				
2	*LDO1_DBN_TLF*	Debounce falling edge programmability: 000: none 001: 2 μs 010: 4 μs 011: 8 μs 100: 16 μs 101: 32 μs 110: 64 μs 111: 128 μs		
1				
0				

Table 58. MONITORING OVERVOLTAGE LDO1 SETTINGS

Register Name		MONITORING_OV_LDO1	Address	2C
Type		CRC	Default	01010000b (50h)
Trigger				
Bit	**Name**	**Description**		
7	*LDO1_OVT*	LDO1 Under Voltage Monitoring Threshold in % of the programmed output voltage: 000: 3.0% 001: 3.5% 010: 4.0% 011: 4.5% 100: 5.0% 101: 6.0% 110: 8.0% 111: 10%		
6				
5				
4	*LDO1_DBN_THR*	Debounce rising edge programmability: 000: none 001: 2 μs 010: 4 μs 011: 8 μs 100: 16 μs 101: 32 μs 110: 64 μs 111: 128 μs		
3				
2				
1	*LDO1_DBN_THF*	Debounce falling edge programmability: 00: 32 μs 01: 64 μs 10: 128 μs 11: 256 μs		
0				

Table 59. SEQUENCER ASSIGNMENT DCDC1 REGISTER

Register Name		SEQUENCER_ASSIGNMENT_DCDC1	Address	2D
Type		CRC	Default	00000000b (0h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	*SLOTPDS_DCDC1*	DCDC1 Power Down Sequence SLOT assignment		
4				
3	empty			
2	empty			
1	*SLOTPUS_DCDC1*	DCDC1 Power up Sequence SLOT assignment		
0				

Table 60. SEQUENCER ASSIGNMENT DCDC2 REGISTER

Register Name		SEQUENCER_ASSIGNMENT_DCDC2	Address	2E
Type		CRC	Default	00010001b (11h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	*SLOTPDS_DCDC2*	DCDC2 Power Down Sequence SLOT assignment		
4				
3	empty			
2	empty			
1	*SLOTPUS_DCDC2*	DCDC2 Power up Sequence SLOT assignment		
0				

Table 61. SEQUENCER ASSIGNMENT DCDC3 REGISTER

Register Name		SEQUENCER_ASSIGNMENT_DCDC3	Address	30
Type		CRC	Default	00100010b (22h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	*SLOTPDS_DCDC3*	DCDC3 Power Down Sequence SLOT assignment		
4				
3	empty			
2	empty			
1	*SLOTPUS_DCDC3*	DCDC3 Power up Sequence SLOT assignment		
0				

Table 62. SEQUENCER ASSIGNMENT LDO1 REGISTER

Register Name		SEQUENCER_ASSIGNMENT_LDO1	Address	31
Type		CRC	Default	00110011b (33h)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	empty			
5	*SLOTPDS_LDO*	LDO1 Power Down Sequence SLOT assignment		
4				
3	empty			
2	empty			
1	*SLOTPUS_LDO*	LDO1 Power up Sequence SLOT assignment		
0				

Table 63. SEQUENCER CONFIGURATION REGISTER 1

Register Name		SEQUENCER_CONFIGURATION_1	Address	32
Type		CRC	Default	00001101b (Dh)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	*PUS_Init_Delay*	Power Up Sequence Init Delay at the beginiing of SLOTx 00: 0 μs 01: 128 μs 10: 256 μs 11: 1024 μs		
5				
4	*PUS_DELAY*	PUS_Init_Delay assignment: 0: only SLOT 0 1: All SLOT		
3	*PUSTO*	Time period of empty slot, power up sequence fault for assigned slot 00: 2 ms 01: 4 ms 10: 8 ms 11: 16 ms		
2				
1	*RST_DLY*	Power up Sequence Reset Delay (/RST pin) 00: 2 ms 01: 8 ms 10: 16 ms 11: 32 ms		
0				

Table 64. SEQUENCER CONFIGURATION REGISTER 2

Register Name		SEQUENCER_CONFIGURATION_2	**Address**	33
Type		CRC	**Default**	01101011b (6Bh)
Trigger				
Bit	**Name**	**Description**		
7	empty			
6	*PDS_Init_Delay*	Power Down Sequence Init Delay 00: 128 μs 01: 512 μs 10: 2048 μs 11: 8192 μs		
5				
4	empty			
3	*PDSTO*	Time period of empty slot, no power down sequence fault for assigned slot (continues to next slot once delay is reached) 00: 4 ms 01: 8 ms 10: 16 ms 11: 32 ms		
2				
1	PWR_SEQ_EN	Bit to enable / disable the internal sequencer: 0: disabled (internal regulator controlled by ENx bits) 1: enabled		
0	PS	0: start the power down sequence 1: start the power up sequence		

APPLICATION INFORMATION

Output Filter Design Considerations

The output filter introduces a double pole in the system at a frequency of

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C}} \quad \text{(eq. 7)}$$

The internal compensation network design of the NCV92310 is optimized for the typical output filter.

Inductor Selection

The inductance of the inductor is determined by given peak−to−peak ripple current I_{L_PP} of approximately 20% to 50% of the maximum output current I_{OUT_MAX} for a trade−off between transient response and output ripple. The inductance corresponding to the given current ripple is

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{L\_PP}} \quad \text{(eq. 8)}$$

The selected inductor must have high enough saturation current rating to be higher than the maximum peak current that is

$$I_{L\_MAX} = I_{OUT\_MAX} = \frac{I_{L\_PP}}{2} \quad \text{(eq. 9)}$$

The inductor also needs to have high enough current rating based on temperature rise concern. Low DCR is good for efficiency improvement and temperature rise reduction. Table 65 shows some recommended inductors for high power applications and Table 65 shows some recommended inductors for low power applications.

Table 65. LIST OF RECOMMENDED INDUCTORS

Manufacturer	Part #	Case Size (mm)	L (μH)	Rdc (Ω) Typ / Max	Rac (Ω)	Rated Current (mA) (Inductance Drop)
MURATA	DFE2HCAH2R2MJ0	2520	2.2	84 / 101	0.85	3100
TDK	TFM252012ALMA2R2MTAA	2520	2.2	75 / 84	1.14	3300
MURATA	DFE2MCAH1R0MJ0	2016	1.0	57 / 68	0.48	3100
TDK	TFM201610ALMA1R0MTAA	2016	1.0	50 / 60	0.54	3700
TDK	TFM201612BLEA1R0MTCA	2016	1.0	34 / 42	–	4300
TDK	TFM201612BLEA2R2MTCA	2016	2.2	80 / 105	–	2800

Output Capacitor Selection

The output capacitor selection is determined by output voltage ripple and load transient response requirement. For a given peak−to−peak ripple current IL_PP in the inductor of the output filter, the output voltage ripple across the output capacitor is the sum of three ripple components as below

$$V_{OUT\_PP} \approx V_{OUT\_PP(C)} + V_{OUT\_PP(ESR)} + V_{OUT\_PP(ESL)} \quad \text{(eq. 10)}$$

Where $V_{OUT\_PP(C)}$ is a ripple component by an equivalent total capacitance of the output capacitors, $V_{OUT\_PP(ESR)}$ is a ripple component by an equivalent ESR of the output capacitors, and $V_{OUT\_PP(ESL)}$ is a ripple component by an equivalent ESL of the output capacitors. In PWM operation mode, the three ripple components can be obtained by

$$V_{OUT\_PP(C)} = \frac{I_{L\_PP}}{8 \times C \times f_{SW}} \quad \text{(eq. 11)}$$

$$V_{OUT\_PP(ESR)} = I_{L\_PP} \times ESR \quad \text{(eq. 12)}$$

$$V_{OUT\_PP(ESL)} = \frac{ESL}{ESL + L} \times V_{IN} \quad \text{(eq. 13)}$$

And the peak−to−peak ripple current is

$$I_{L\_PP} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L} \quad \text{(eq. 14)}$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is $V_{OUT\_PP(C)}$. So that the minimum output capacitance C_{OUT_MIN} can be calculated regarding to a given output ripple requirement V_{OUT_PP} in PWM operation mode.

$$C_{OUT\_MIN} = \frac{I_{L\_PP}}{8 \times V_{OUT\_PP} \times f_{SW}} \quad \text{(eq. 15)}$$

Input Capacitor Selection

One of the input capacitor selection guides is the input voltage ripple requirement. To minimize the input voltage ripple and get better decoupling in the input power supply rail, ceramic capacitor is recommended due to low ESR and ESL. The minimum input capacitance C_{IN_MIN} regarding to the input ripple voltage V_{IN_PP} is

$$C_{IN\_MIN} = \frac{I_{OUT\_MAX} \times (D - D^2)}{V_{IN\_PP} \times f_{SW}} \quad \text{(eq. 16)}$$

Where

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 17)}$$

In addition, the input capacitor needs to be able to absorb the input current, which has an RMS value of

$$I_{IN\_RMS} = I_{OUT\_MAX} \times \sqrt{D - D^2} \quad \text{(eq. 18)}$$

The input capacitor also needs to be sufficient to protect the device from over voltage spike, and normally at least a 4.7 μF capacitor is required. The input capacitor should be located as close as possible to the IC on PCB.

Table 66. LIST OF RECOMMENDED INPUT AND OUTPUT CAPACITORS

Manufacturer	Part #	Case Size (mm)	Technology	C (μF)	Rated Voltage (V)
TDK	CGA5L1X7R1E106K160AC	1206	X7R	10	25
Murata	GCM31CC71E106KA03L	1206	X7S	10	25
TDK	CGA4J1X7S1E106K125AC	0805	X7S	10	25
TDK	CGA4J1X7R0J106K125AC	0805	X7R	10	6.3
Murata	GCM21BR71A106KE22L	0805	X7R	10	10
TDK	CGA3E1X7T0J106M080AC	0603	X7T	10	6.3
TDK	CGA3E1X7R0J225K080AC	0603	X7R	2.2	6.3
TDK	CGA2B3X7R1E224K050BB	0402	X7R	0.22	50
TDK	CGA2B3X7R1E104K050BB	0402	X7R	0.1	25
TDK	CGA2B3X7R1E474K050BB	0402	X7S	0.47	10
MURATA	GCM155C71A105K	0402	X7S	1	10

PCB LAYOUT CONSIDERATIONS

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- Use wide and short traces for power paths (such as P_{VIN}, V_{OUT}, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- The device should be well decoupled by input capacitor and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission.
- SW node should be a large copper pour, but compact because it is also a noise source.
- It would be good to have separated local ground planes for PGND and AGND. Directly connect AGND pin to the exposed pad and then connect to AGND ground plane through vias. Try best to avoid overlap of input ground loop and output ground loop to prevent noise impact on output regulation.
- Arrange a “quiet” path for output voltage sense, and make it surrounded by a ground plane.

To be updated

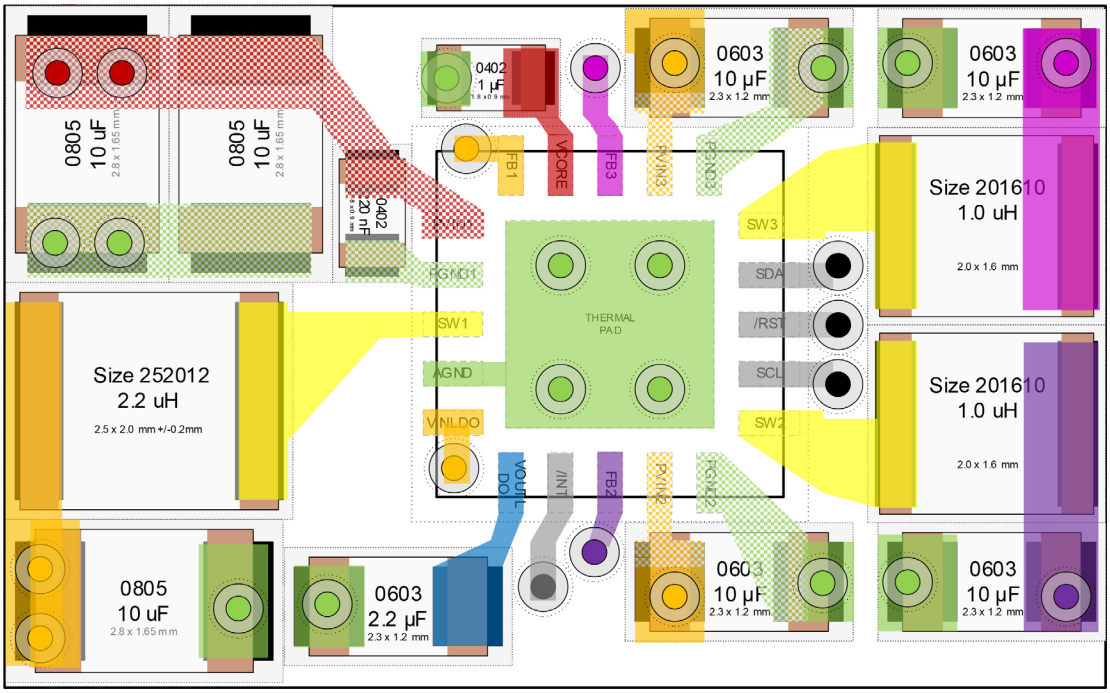

Figure 25. Recommended PCB Layout

ORDERING INFORMATION

Device	Package	Shipping†
NCV92310ABMTWTXG	QFNW20	3000 / Tape & Reel
TBD	TBD	TBD / Tape & Reel
TBD	TBD	TBD / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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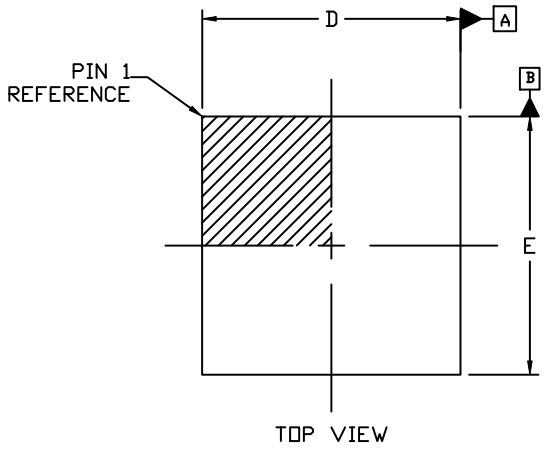
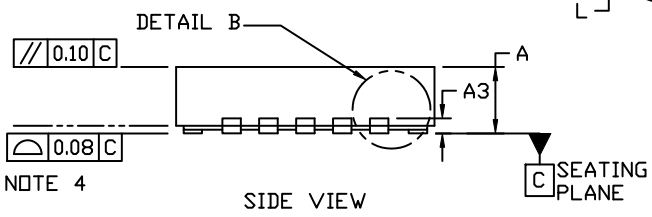
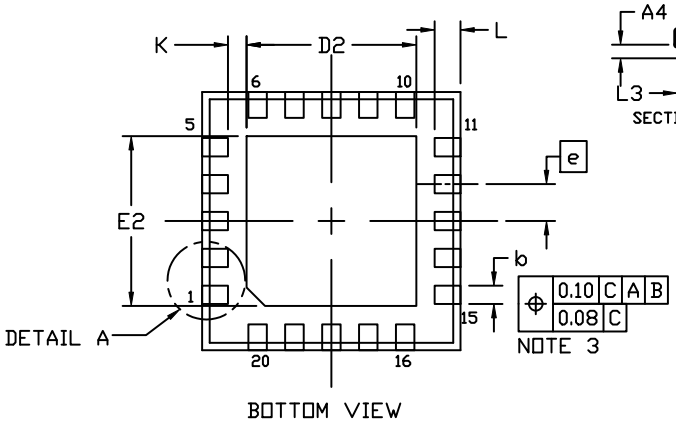
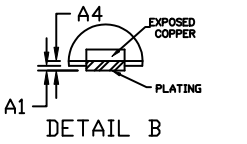
PACKAGE DIMENSIONS

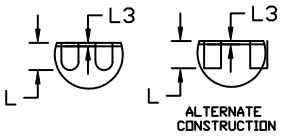
QFNW20 3.5x3.5, 0.5P
CASE 484AV
ISSUE A

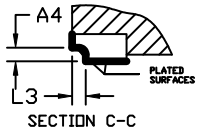








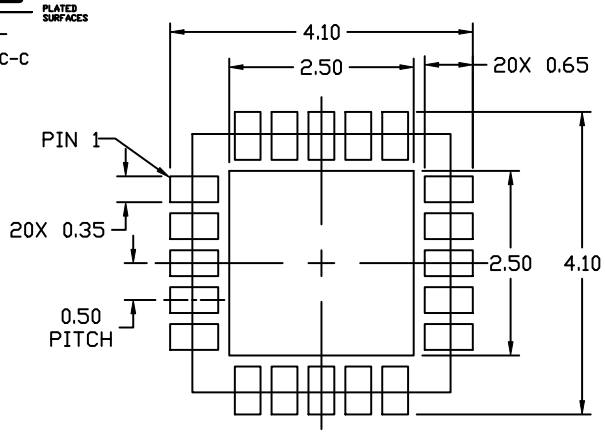




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.20	0.25	0.30
D	3.40	3.50	3.60
D2	2.20	2.30	2.40
E	3.40	3.50	3.60
E2	2.20	2.30	2.40
e	0.50 BSC		
k	0.25 REF		
L	0.25	0.35	0.45
L3	---	---	0.09



RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

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