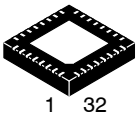
Automotive Ethernet Transceiver (MAC-PHY) 10BASE-T1S MultiDrop

NCV7410



QFNW32 5x5, 0.5P
CASE 484AB

MARKING DIAGRAM

V7410	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 64 of this data sheet.

Description

The NCV7410 device is an IEEE 802.3cg−compliant Ethernet Transceiver with an integrated Media Access Controller (MAC−PHY).

The NCV7410 can communicate with multiple nodes connected to a shared medium (UTP) at 10 Mbps. It consists of CSMA/CD MAC and PHY with Physical Layer Collision Avoidance (PLCA). PLCA prevents collisions at the physical layer and, therefore, improves the throughput of CSMA/CD. The NCV7410 uses SPI (with a clock up to 25 MHz) as an interface to host MCU.

Features

- Compliant to IEEE 802.3cg 2019
  - Supports Half−Duplex, Multidrop Mode
- Physical Layer Collision Avoidance (PLCA)
- SPI Interface (OPEN Alliance 10BASE−T1x MAC−PHY Serial Interface)
- Distance Measurement between Nodes
- Single 3.3 V Supply Operation
- Transmitter Optimized for Capacitive Coupling to UTP Cable
- MDI Pins Protected against:
  - ±6 kV ESD (HBM, IEC61000−4−2)
  - Transient Pulses (ISO7637)
- Operating Ambient Temperature −40°C to +125°C (T_{AMB_Class1})
- Junction Temperature Range −40°C to +150°C

Environment

- These are Pb−Free Devices

Typical Applications

- Automotive
- Agricultural Machinery
- Machine Control

Quality

- Wettable Flank Package for Enhanced Optical Inspection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

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APPLICATION INFORMATION

Figure 1 shows an example of an application with the NCV7410.

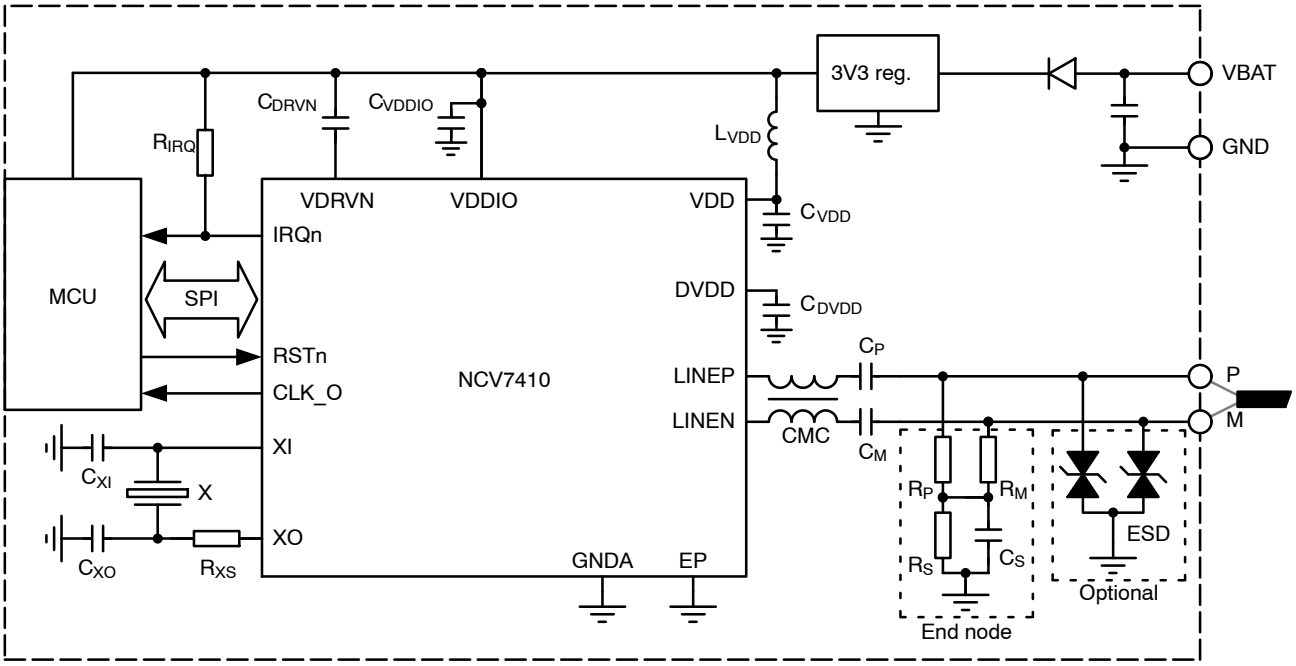


Figure 1. Basic Application Diagram

Table 1. RECOMMENDED EXTERNAL COMPONENTS FOR THE APPLICATION DIAGRAM

Component	Function	Value	Unit	Note
C_{VDD}	Filtering Capacitor, Ceramic	2.2	μF	
L_{VDD}	Analog Power Supply Ferrite	1	kΩ	Measured at 100 MHz
C_{VDDIO}	Filtering Capacitor, Ceramic	100	nF	
C_{DRVN}	Filtering Capacitor, Ceramic	2.2	μF	
C_{DVDD}	Filtering Capacitor, Ceramic	2.2	μF	
R_{IRQ}	IRQ Pull Up Resistor	10	kΩ	
X	Crystal (e.g. Murata XRCGB25M000F3A00R0)	25	MHz	±100 ppm
R_{XS}	Series Resistor	0	Ω	
C_{XI}, C_{XO}	Load Capacitors	Depends on used crystal	pF	
CMC	Common Mode Choke (e.g. TDK ACT1210E−241−2P)	240	μH	
C_P,C_M	DC−blocking Coupling Capacitors	100	nF	<10%, 50 V
R_P, R_M	Terminating Resistors	49.9	Ω	<1%, ≥0.4 W
C_S	Capacitor	4.7	nF	<10%, 50 V
R_S	Resistor	100	kΩ	<10%, ≥0.1 W
ESD	ESD Protection	SZESD9902 / 9901		Optional

BLOCK DIAGRAM

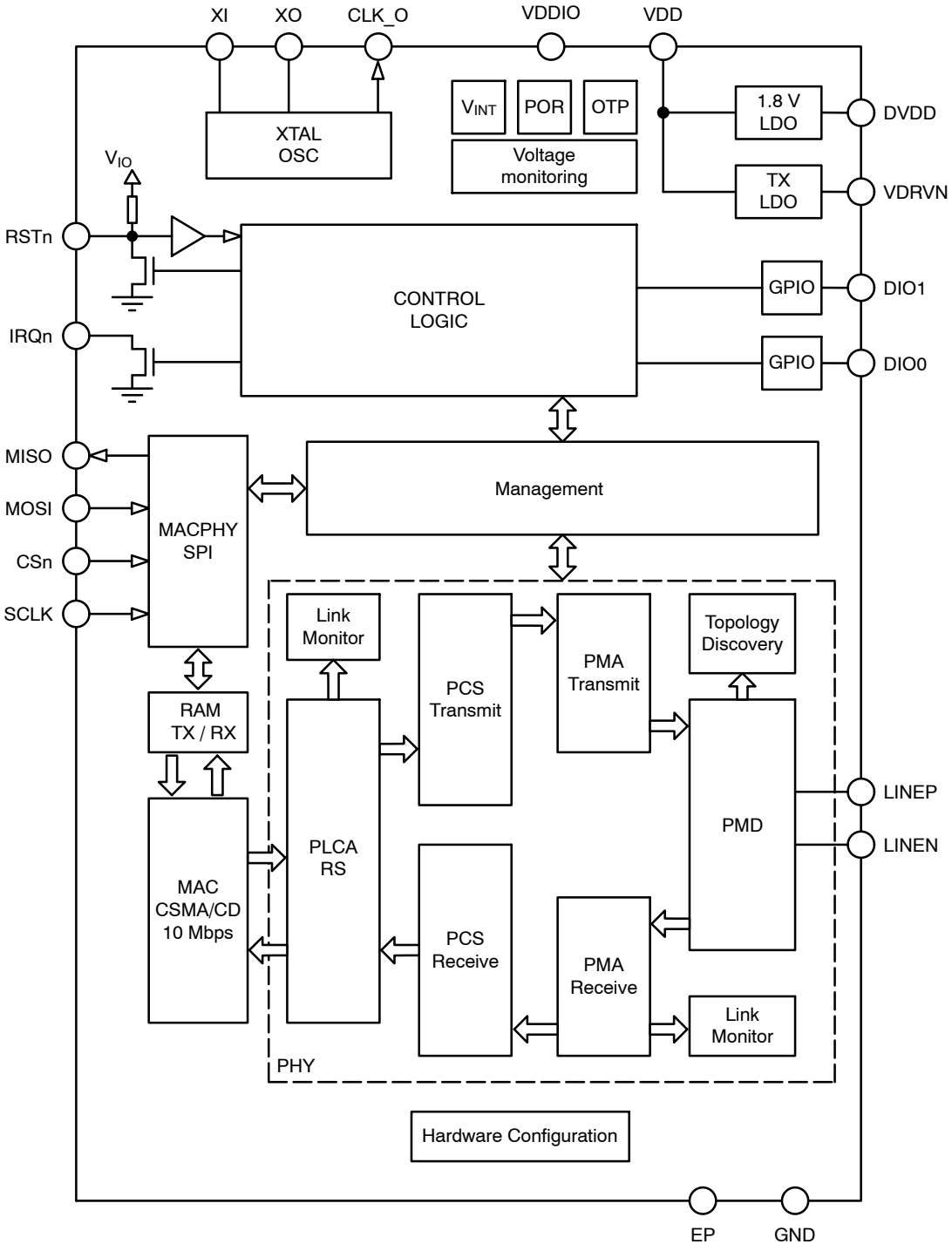


Figure 2. Block Diagram

PIN ASSIGNMENT

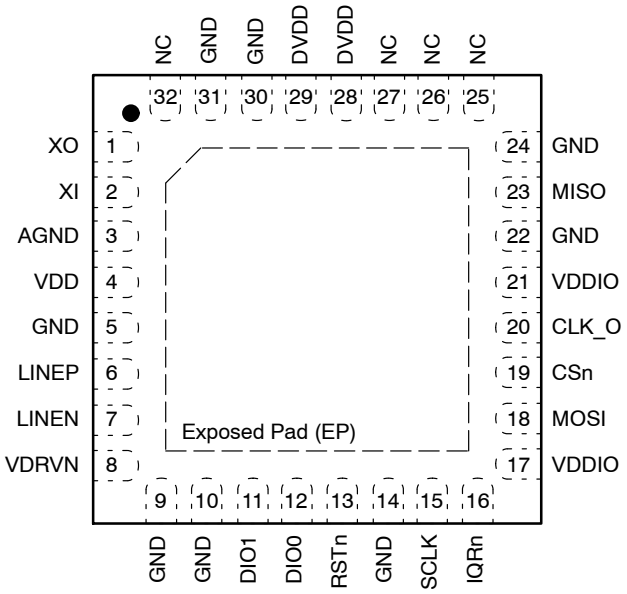


Figure 3. Pin Assignment – QFN32 (Top View)

PIN DEFINITION

The pinout of the NCV7410 is shown in Figure 3. The pin list is given in Pin Function Description table below.

Table 2. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Function	Description
1	XO	Output	Crystal XO
2	XI	Input	Crystal XI / Reference clock input
4	VDD	Power Supply	3.3 V Power Supply Input
6	LINEP	Analog Input / Output	Positive Medium Dependent Interface (MDI) terminal
7	LINEN		Negative Medium Dependent Interface (MDI) terminal
8	VDRVN	Supply (regulator output)	Output of internal TX LDO. Proper decoupling needed.
11	DIO1	GPIO	General Purpose IO. During BOOT, an internal pull−down is connected to both DIOs. See DIO Configuration Register.
12	DIO0		
13	RSTn	Digital Input, Open Drain	Reset pin (Active−low), internal 54 kΩ pull−up, driven low (25 Ω) during undervoltage event. To prevent damage, when driving this from an MCU or any active driver, make sure that such drive is configured to be an open drain driver.
15	SCLK	Digital Input	SPI interface Shift Clock
16	IRQn	Digital Output, open drain	Interrupt pin, active low
17, 21	VDDIO	Supply Input	Digital I/O voltage reference (3.3 V or 2.5 V)
18	MOSI	Digital Input	SPI interface Serial Data Input
19	CSn		SPI interface Chip Select (active low)
20	CLK_O	Digital Output	25 MHz clock output
23	MISO	Digital Output	SPI interface Serial Data Output
25, 26, 27	NC	Reserved	Do not connect
28, 29	DVDD	Supply (regulator output)	Output of internal 1.8 V LDO. Proper decoupling is needed.
32	NC	Reserved	Do not connect
3, 5, 9, 10, 14, 22, 24, 30, 31	GND	Ground	Connect to GND in the application
EP	Exposed Pad		

Table 3. MAXIMUM RATINGS

Symbol	Rating	Min	Max	Unit
V_{VDD_MAX}	Voltage Supplies (VDD, VDDIO), (Note 1)	−0.3	3.65	V
V_{DVDD_MAX}	Low Voltage Supply Output (DVDD)	−0.3	1.98	V
V_{LINE_MAX}	Voltage on LINE Pins	−30	30	V
V_{DIGIN_MAX}	Digital Input Pins	−0.3	VDDIO + 0.3	V
V_{DIGOUT_MAX}	Digital Output Pins	−0.3	VDDIO + 0.3	V
I_{DIGOUT_MAX}	Current on Digital Output Pins	−	20	mA
V_{GND_MAX}	Ground Pins (GND)	−0.3	0.3	V
V_{TRAN}	Voltage Transients, Pins LINEP, LINEN per ISO7637 Part 3	−150	100	V
ESD_{System_HBM}	On Pins LINEP, LINEN (Note 2)	>±6		kV
$ESD_{Component\_HBM}$	Human Body Model on Pins LINEP, LINEN (Note 3)	>±8		kV
$ESD_{Component\_HBM}$	Human Body Model on All Pins (Note 4)	>±2		kV
ESD_{CDM}	Charge device Model on All Pins as per JESD22−C101 / AEC−Q100−011	>±500		V
LU	Static Latch−up Measured on All Pins per EIA/JESD78	−100	100	mA
T_{STG}	Storage Temperature	−65	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. As per IEC 61000−4−2, 330 Ω / 150 pF
3. Stressed towards GND as per JESD22−A114 / AEC−Q100−002, 1500 Ω / 100 pF
4. As per JESD22−A114 / AEC−Q100−002

Table 4. RECOMMENDED OPERATING RANGES

Symbol	Rating	Min	Max	Unit
VDD	Voltage Supply at VDDA and VDD	2.97	3.63	V
VDDIO	Voltage Supply (VDDIO) for Digital IO	2.25	3.63	V
DigIO	DC Voltage at Digital Pins	0	VDDIO	V
T_{AMB}	Ambient Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (VDD = 2.97 V to 3.63 V; VDDIO = 2.25 V to 3.63 V; C_{VDD}, C_{VDDA}, C_{DRVN} = 2.2 μF; C_{VDDIO} = 100 nF; T_J = −40 to +150°C; for typical values T_J = 25°C; for min/max values. T_J = −40 to 150°C; unless otherwise noted. All voltages are referenced to GND (Exposed Pad). Positive currents flow into the respective pin.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
POWER SUPPLY – PIN VDD						
I_{VDD}	Supply Current	Transmitting	–	45	55	mA
		Receiving	–	20	–	mA
		Standby	–	13	–	mA
V_{uvd_VDD}	Undervoltage Detection Threshold	VDD falling	2.42	–	–	V
V_{uvr_VDD}	Undervoltage Recovery Threshold	VDD rising	–	–	2.89	V
	Undervoltage Threshold Hysteresis		95	100	121	mV
	Undervoltage Deglitch Time		4	7	15	μs
POWER SUPPLY – PIN VDDIO						
I_{VDDIO}	Supply Current	Transmitting	–	2	4	mA
		Receiving	–	2	4	mA
		Standby	–	2	4	mA
V_{uvd_VDD}	Undervoltage Detection Threshold	VDDIO falling	1.83	–	–	V
V_{uvr_VDD}	Undervoltage Recovery Threshold	VDDIO rising	–	–	2.17	V
	Undervoltage Threshold Hysteresis		70	80	90	mV
	Undervoltage Deglitch Time		5	10	20	μs
PMA ELECTRICAL MEASUREMENTS – MDI / BUS LINES						
TX_{DROOP}	Transmitter Output Droop (Test Mode 2)	100 * $\lvert V_{DROOP} / V_{PK} \rvert$	–	–	+30	%
t_{TJ}	Transmitter Timing Jitter – Symbol−to−Symbol	Test mode 1	–	–	5	ns
V_{PD}	Transmitter Distortion (Test mode 4)		–	–	15	mV
P_{PSD}	Transmitter Power Spectral Density at Frequency f (MHz) (Test Mode 3)	0.3 MHz ≤ f < 5 MHz	Max. −61			dBm/Hz
		5 MHz ≤ f < 10 MHz	Min. −87 + 2f Max. −61			
		10 MHz ≤ f < 15 MHz	Min. −47 − 2f Max. −61			
		15 MHz ≤ f ≤ 25 MHz	Max. −40 − 1.4f			
		25 MHz ≤ f ≤ 40 MHz	Max. −75			
f_{TR}	Symbol Transmission Rate		–	12.5	–	MBd
f_{TR_Tol}	Symbol Transmission Rate Tolerance		−100	–	100	ppm
a_{RL_Sdd11}	MDI Return Loss at Frequency f (MHz) – Applicable for Point−to−Point Link Segment	0.3 MHz ≤ f ≤ 10 MHz	14	–	–	dB
		10 MHz ≤ f ≤ 40 MHz	Min. $14 - 10 \times \log_{10}\left(\frac{f}{10}\right)$			dB
a_{LCL_Sdc11}	MDI Mode Conversion Loss at Frequency f (MHz) – Applicable for Point−to−Point Link Segment	0.3 MHz ≤ f ≤ 20 MHz	43	–	–	dB
		20 MHz ≤ f ≤ 200 MHz	Min. $43 - 20 \times \log_{10}\left(\frac{f}{20}\right)$			dB
BER	Receiver Bit Error Rate		–	–	10^{-10}	–
BER_ACNR	Bit Error Rate under Alien Crosstalk Noise Injection (with Magnitude of −101 dBm/Hz)	Noise source: Gaussian signal generator with a bandwidth of 40 MHz	–	–	10^{-10}	–

ELECTRICAL CHARACTERISTICS (VDD = 2.97 V to 3.63 V; VDDIO = 2.25 V to 3.63 V; C_{VDD}, C_{VDDA}, C_{DRVN} = 2.2 μF; C_{VDDIO} = 100 nF; T_J = −40 to +150°C; for typical values T_J = 25°C; for min/max values. T_J = −40 to 150°C; unless otherwise noted. All voltages are referenced to GND (Exposed Pad). Positive currents flow into the respective pin.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
MDI TRANSMITTER (VDD = 3.3 V)						
V_{TRX_DIFF}	Transmitter Peak Differential Output Voltage	R_{LOAD} = 50 Ω, Default settings	0.9	1.0	1.1	V
R_{DRIVER}	Bus Driver Output Resistance		40	50	63	Ω
MDI RECEIVER (VDD = 3.3 V)						
R_{REC_IN}	Differential Input Resistance		25	40	60	kΩ
C_{REC_IN}	Differential Input Capacitance	At 20 MHz		5.5	7.5	pF
V_{REC_CM}	Common Mode Voltage Range		−20	–	20	V
V_{REC_TH}	Receiver Threshold		−15	0	15	mV
V_{REC_ED}	Energy Detection Threshold (Default Value, See PHY Configuration 0 Register)	Def. value, see RX_DT	–	±250	–	mV
V_{REC_CD}	Collision Detection Threshold (Default Value, See PHY Configuration 0 Register)	Def. value, see RX_CD	–	±700	–	mV
V_{REC_ACC}	Threshold Accuracy		−30	–	30	mV
DIGITAL IO PINS						
V_{IL}	Low−level Input Voltage	VDDIO = 2.5 V to 3.3 V	–	–	0.7	V
V_{IH}	High−level Input Voltage		2	–	VDDIO	V
V_{OL}	Low−level Output Voltage		–	–	0.45	V
V_{OH}	High−level Output Voltage		VDDIO − 0.45	–	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SPI INTERFACE TIMING

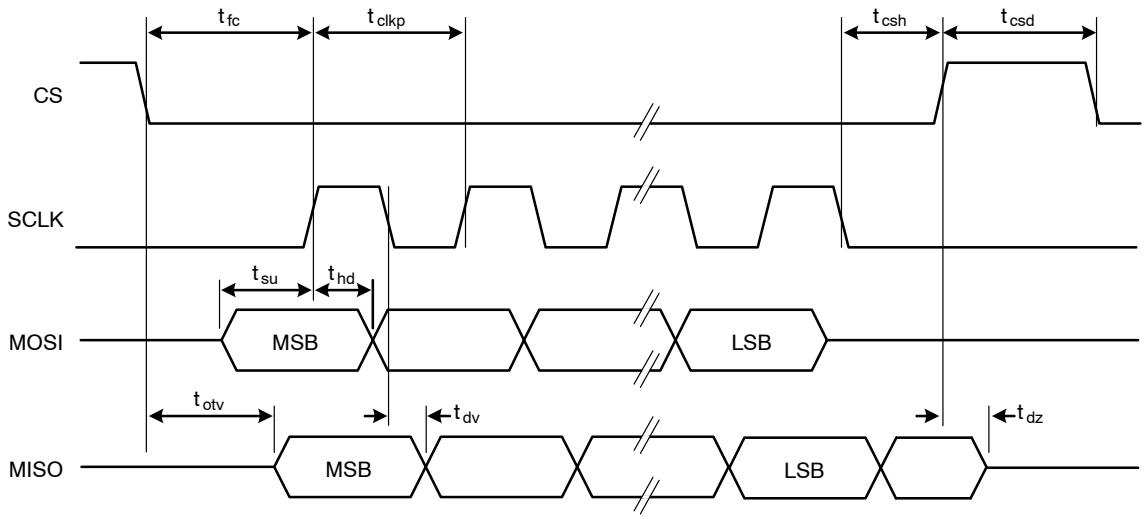


Figure 4. SPI Interface AC Timing Diagram

Table 5. SPI TIMING CHARACTERISTICS

Symbol	Item	Condition	Min	Typ	Max	Unit
t_{clkp}	SPI Clock Period	VDDIO = 2.5 V ±10%	50	–	–	ns
		VDDIO = 3.3 V ±10%	40	–	–	ns
t_{su}	Data Input Setup Time	VDDIO = 2.25 – 3.63 V	8	–	–	ns
t_{hd}	Data Input Hold Time	VDDIO = 2.25 – 3.63 V	5	–	–	ns
t_{dv}	Output Data Valid	VDDIO = 2.5 V ±10%	–	–	14.5	ns
		VDDIO = 3.3 V ±10%	–	–	12	ns
t_{otv}	CS Low to MISO Out Valid	VDDIO = 2.5 V ±10%	–	–	14.5	ns
		VDDIO = 3.3 V ±10%	–	–	12	ns
t_{fc}	CS Low to Rising Edge of SCLK	VDDIO = 2.25 – 3.63 V	20	–	–	ns
t_{csh}	SCLK Falling to CS De−assert	VDDIO = 2.25 – 3.63 V	5	–	14.5	ns
t_{dz}	CS De−assert to MISO HIGH−Z	VDDIO = 2.5 V ±10%	–	–	14.5	ns
		VDDIO = 3.3 V ±0%	–	–	12	ns
t_{csd}	Minimum CS De−assertion Time	VDDIO = 2.25 – 3.63 V	350	–	–	ns

DETAILED DESCRIPTION

The NCV7410 is a 10BASE−T1S Physical Layer Transceiver as specified in IEEE 802.3cg with an integrated Media Access Controller (MAC). It supports operation over a shared media (multidrop) network with up to 25 m of a single twisted pair (UTP / STP) connection.

The NCV7410 provides a Serial Peripheral Interface (SPI) in slave mode, allowing low pin count connection to standard, off−the−shelf Microcontrollers or SoC. The NCV7410 provides a link speed of 10 Mbit/s in half−duplex operation.

The MAC−PHY's SPI protocol is compliant to the specification issued by the Open Alliance. The NCV7410 can be locally configured to run Physical Layer Collision Avoidance (PLCA), that supports at least 8 nodes on the shared medium, depending on environmental conditions.

PLCA improves data throughput under high network load and provides additional benefits:

- Nodes are granted transmit opportunities using a round−robin arbitration scheme, enabling fair−shared access to the medium.
- By avoiding multiple back−off and retry events in the embedded MAC, maximum latencies are significantly reduced.
- Protects against the "babbling idiot" problem, as a single station can only transmit when granted an opportunity to do so.

The integration of the PLCA reconciliation sublayer (PLCA RS) in the device enables connected hosts to take full advantage of collision−free Ethernet communication on a single twisted pair, shared medium.

The integrated CSMA/CD 10 Mbps MAC provides the following features:

- Multiple MAC address filtering
- Broadcast / Multicast filtering
- Promiscuous Mode, accepting every frame regardless of its type or address
- FCS generation / checking
- Statistics / Diagnostic Counters
- Status reporting
- Factory provided unique MAC address.

The SPI Protocol handler supports:

- 8−byte, 16−byte, 32−byte and 64−byte data chunks
- Both "Store & Forward" and "Cut−Through" operation
- Protected and Unprotected control transaction
- 4 kB TX−Buffer
- 4 kB RX−Buffer
- SPI clock up to 25 MHz

Additional non−standard features are implemented into the NCV7410:

- Enhanced Noise Immunity PMA operation (ENI)
- Collision detection masking
- PLCA Precedence Mode
- PLCA coordinator selection
- Proprietary topology discovery, allowing to measure the distance between nodes on the link segment − works only when all communication partners are **onsemi** 10BASE−T1S devices: NCV7410, NCV7311, NCN26010 or NCN26000.

The integrated Crystal Oscillator circuitry allows the use of an external CMOS oscillator, a quartz crystal, or any other external clock source, as long as its accuracy is in line with the specifications.

OPERATING MODES

General

The NCV7410 offers two operation modes, that can be selected using strap pin DIO0 during BOOT (reset or power up), NORMAL mode, and ISOLATED mode.

NORMAL Mode

In NORMAL mode the NCV7410 works as a standard 10BASE−T1S MAC−PHY, connecting to the host via an SPI interface.

ISOLATED Mode

In ISOLATED mode, LINEP and LINEN pins are held in high impedance mode, SPI interface and DIO pins work as in NORMAL mode.

To move from ISOLATED mode to NORMAL operation, the ISOM bit in the PHY Control Register needs to be cleared.

BOOT

When the RST pin is de−asserted or upon Power ON Reset, the NCV7410 enters BOOT mode. In BOOT mode, all interface pins are either inputs or tri−stated outputs. After the mode pin (DIO0) is sampled, the NCV7410 enters either NORMAL or ISOLATED mode and all interface pins are re−configured accordingly.

The open−drain IRQn pin signals finished boot by a short low pulse (typical duration: 160 ns). If the CS signal is high after the reset, IRQn stays low due to a non−maskable Reset Complete (RESETC) interrupt.

Table 6. BOOTSTRAPS PIN

Pin Name	Bootstrap Function	Description
DIO0	ISOLATE	Selects the operation mode: 0 = NORMAL mode 1 = ISOLATED mode Internal Pull−Down connected during BOOT.

DIO0 can be set to High or Low, using an external device or a pull resistor in the range between 1 kΩ and 10 kΩ.

POWER−OFF Mode

The NCV7410 remains in POWER−OFF mode as long as the voltage at any supply pin (VDD, DVDD, or VDDIO) is below its undervoltage recovery threshold. POWER−OFF mode is also entered from any other operating mode in case of undervoltage detection.

As soon as the voltage at all supply pins rises above the undervoltage recovery threshold, POR is issued, all registers are reset to their default values, and the NCV7410 proceeds to BOOT.

REGISTER MEMORY MAP

The NCV7410 provides the registers grouped in memory map selection groups. See the below table for details.

Table 7. MEMORY MAP SELECTION GROUP

MMS	Width	Memory Map Description
0	32	Standard SPI Control and Status, PHY MIIM (Clause 22)
1	32	MAC Registers
2	16	PHY– PCS Registers (IEEE802.3 MMD3)
3	16	PHY– PMA/PCS Registers (IEEE802.3 MMD 1)
4	16	PHY – PCLA and Vendor–specific Registers (MMD 31)

The OA–SPI protocol always treats registers as 32–bit. Registers that are 16–bit wide will have the two most significant bytes read as 0x00. For write commands to 16–bit registers, the two most significant bytes are ignored.

Each register is defined by a table containing the following attributes:

- MMS: The target MMS that together with ADDR uniquely identifies the register
- Address: The 16–bit target address within the specified MMS at which the register can be accessed
- Default: The initial value of the register after a reset

In the same table, each bit–field is further qualified by the following attributes:

- Bit(s): The bit number/range at which the field is located within the register
- Name: The name of the field
- Description: A short description of the field
- Default: The initial value of the field after a reset
- Access: The allowed access type of the field, as specified in Table 7

Table 8. DESCRIPTION OF REGISTER FIELD ACCESS TYPES USED IN THIS DOCUMENT

Access	Memory Map Description
RW	The field can be read from and written to
RO	The field is read–only. Writes to a RO field are ignored. If a default value is present, then the field is a constant
RO–SCR	Read–only field that self–clears on read.
R/W1C	Read–only field that can be cleared by writing a 1 to it.
RW–SC	Read–Write filed, whose content is cleared to its default values after the underlying operation is completed.
RO–LH	Read–only, Latch high on the occurrence of the underlying event. Clears on read.

Table 9. REGISTER MAP OVERVIEW

MMS		Address		Name
Hex	Dec	Hex	Dec	
MMS0 REGISTERS				
0x0	0	0x0	0	SPI Identification Register, IDVER
		0x1	1	SPI Identification Register, PHY ID
		0x2	2	SPI Capabilities, SPICAP
		0x3	3	Reset Control and Status, RESET
		0x4	4	SPI Protocol Configuration Register, CONFIG0
		0x8	8	SPI Protocol Status Register, STATUS0
		0xB	11	Buffer Status Register, BUFSTS
		0xC	12	Interrupt Mask Register, IMASK
		0xFF00	65280	PHY Control Register
		0xFF01	65281	PHY Status Register
		0xFF02	65282	PHY Identifier 0 Registers
		0xFF03	65283	PHY Identifier 1 Registers
MMS1 REGISTERS – REGISTERS RELATED TO THE MAC				
0x1	1	0x0	0	MAC Control0 Register
		0x10	16	Address Filter 0 Low, ADDRFILT0L
		0x11	17	Address Filter 0 High, ADDRFILT0H
		0x12	18	Address Filter 1 Low, ADDRFILT1L
		0x13	19	Address Filter 1 High, ADDRFILT1H
		0x14	20	Address Filter 2 Low, ADDRFILT2L
		0x15	21	Address Filter 2 High, ADDRFILT2H
		0x16	22	Address Filter 3 Low, ADDRFILT3L
		0x17	23	Address Filter 3 High, ADDRFILT3H
		0x20	32	Address Mask 0 Low, ADDRMASK0L
		0x21	33	Address Mask 0 High, ADDRMASK0H
		0x22	34	Address Mask 1 Low, ADDRMASK1L
		0x23	35	Address Mask 1 High, ADDRMASK1H
		0x24	36	Address Mask 2 Low, ADDRMASK2L
		0x25	37	Address Mask 2 High, ADDRMASK0H
		0x26	38	Address Mask 3 Low, ADDRMASK3L
		0x27	39	Address Mask 0 High, ADDRMASK3H
		0x30	48	Statistic, Sent Bytes Counter Low, STOCTETSTXL
		0x31	49	Statistic, Sent Bytes Counter High, STOCTETSTXH
		0x32	50	Statistic, Frames Sent Ok, STFRAMESTXOK
		0x33	51	Statistic, Broadcast Frames Sent Ok, STBCASTTXOK
		0x34	52	Statistic, Multicast Frames Sent Ok, STMCASTTXOK
		0x35	53	Statistic, 64−byte Frames Sent Ok, STFRAMESTX64
		0x36	54	Statistic, 65−byte to 127−byte Frames Sent Ok, STFRAMESTX65
		0x37	55	Statistic, 128−byte to 255−byte Frames Sent Ok, STFRAMESTX128
		0x38	56	Statistic, 256−byte to 511−byte Frames Sent Ok, STFRAMESTX256
		0x39	57	Statistic, 512−byte to 1023−byte Frames Sent Ok, STFRAMESTX512

Table 9. REGISTER MAP OVERVIEW (continued)

MMS		Address		Name
Hex	Dec	Hex	Dec	
MMS1 REGISTERS – REGISTERS RELATED TO THE MAC				
0x1	1	0x3A	58	Statistic, 1024−byte or More Frames Sent Ok, STFRAMESTX1024
		0x3B	59	Statistic, Aborted frames Due to TX−buffer Underflow, STUNDERFLOW
		0x3C	60	Statistic, Frames Transmitted after a Single Collision, STSINGLECOL
		0x3D	61	Statistic, Frames Transmitted after Multiple Collisions, STMULITCOL
		0x3E	62	Statistic, Frames Transmitted after Excessive Collisions, STEXCESSCOL
		0x3F	63	Statistic, Frames Transmitted after Deferral, STDEFEEREDTX
		0x40	64	Statistic, Counter of CRS De−assertion During Frame Transmission, STCRSERR
		0x41	65	Statistic, Received Bytes Counter Low, STOCTETSRXL
		0x42	66	Statistic, Received Bytes Counter High, STOCTETSRXH
		0x43	67	Statistic, Frames Received Ok, STFRAMESRXOK
		0x44	68	Statistic, Broadcast Frames Received Ok, STBCASTRXOK
		0x45	69	Statistic, Multicast Frames Received Ok, STMCASTRXOK
		0x46	70	Statistic, 64−byte Frames Received Ok, STFRAMESRX64
		0x47	71	Statistic, 65−byte to 127−byte Frames Received Ok, STFRAMESTX65
		0x48	72	Statistic, 128−byte to 255−byte Frames Received Ok, STFRAMESTX128
		0x49	73	Statistic, 256−byte to 511−byte Frames Received Ok, STFRAMESTX256
		0x4A	74	Statistic, 512−byte to 1023−byte Frames Received Ok, STFRAMESTX512
		0x4B	75	Statistic, 1024−byte or More Frames Received Ok, STFRAMESTX1024
		0x4C	76	Statistic, Dropped Too Short Frames, STRUNTERR
		0x4D	77	Statistic, Dropped Too Long Frames STRXTOOLONG
		0x4E	78	Statistic, Dropped FCS Error Frames STFCSERRS
		0x4F	79	Statistic, Symbol Errors During Frame Reception, STSYMBOLERRS
		0x50	80	Statistic, Align Errors During Frame Reception, STALIGNERRS
		0x51	81	Statistic, RX Buffer Overflow Errors, STRXOVERFLOW
		0x52	82	Statistic, RX Dropped Frame Count, STRXDROPPED
MMS2 REGISTERS – REGISTERS RELATED TO THE PHY: PCS				
0x2	2	0x5	5	Devices in Package 1 Register
		0x6	6	Devices in Package 2 Register
		0x8F3	2291	10BASE−T1S PCS Control Register
		0x8F4	2292	10BASE−T1S PCS Status Register
		0x8F5	2293	10BASE−T1S PCS Diagnostics Register 1
		0x8F6	2294	10BASE−T1S PCS Diagnostics Register 2
MMS3 REGISTERS – REGISTERS RELATED TO THE PHY: PMA				
0x3	3	0x5	5	Devices in Package 1 Register
		0x6	6	Devices in Package 2 Register
		0x12	18	BASE−T1 Extended Ability Register
		0x8F9	2297	10BASE−T1S PMA Control Register
		0x8FA	2298	10BASE−T1S PMA Status Register
		0x8FB	2299	10BASE−T1S Test Mode Control Register

Table 9. REGISTER MAP OVERVIEW (continued)

MMS		Address		Name
Hex	Dec	Hex	Dec	
MMS4 REGISTERS – REGISTERS RELATED TO THE PHY: PLCA				
0x4	4	0x8000	32768	Chip Revision Register
		0x8001	32769	PHY Configuration 1 Register
		0x8002	32770	PLCA Extensions Register
		0x8003	32771	PMA Tune 0 Register
		0x8004	32772	PMA Tune 1 Register
		0xCA00	51712	PLCA Register Map and Identification Register, PLCIDVER
		0xCA01	51713	PCLA Control 0 Register, PLCACTRL0
		0xCA02	51714	PCLA Control 1 Register, PLCACTRL1
		0xCA03	51715	PCLA Status Register, PLCASTATUS
		0xCA04	51716	PCLA Transmit Opportunity Timer Register, PLCATOTMR
		0xCA05	51717	PCLA Burst Mode Register, PLCABURST
MMS12 REGISTERS – VENDOR SPECIFIC REGISTERS				
0xC	12	0x10	16	MIIM Interrupt Control Register
		0x11	17	MIIM Interrupt Status Register
		0x12	18	DIO Configuration Register
		0x16	22	Topology Discovery Control Register
		0x17	23	Topology Discovery Status Register
		0x18	24	Topology Discovery Result Register
		0x19	25	Topology Discovery Precision Register
		0x1A	26	Topology Reference Counter Timer Register
		0x1001	4097	PHY Configuration 0 Register
		0x1002	4098	MACID0
		0x1003	4099	MACID1
		0x1004	4100	Chip Info Register
		0x1005	4101	NVM Health Register

MMS0 REGISTERS

SPI Identification Register, IDVER

MMS: 0
Address: 0x0
Default: 0x11

Bit(s)	Name	Description	Default	Access
31:8	–	Value always 0	0x0	RO
7:4	MAJVER	**Major Version Number**	0x1	RO
3:0	MINVER	**Minor Version Number**	0x1	RO

SPI Identification Register, PHY ID

MMS: 0
Address: 0x1
Default: –

Bit(s)	Name	Description	Default	Access
31:10	OUI	**Organizational Unique Identifier** Records the 22 MSBs of the OUI in reverse order. Bit 31 maps bit 2 of the OUI, bit 10 maps bit 23 of the OUI. Bits 0 and 1 are 0. NOTE: **onsemi**'s OUIs can be found at: https://standards−oui.ieee.org/	–	RO
9:4	MODEL	**Model Number**	0x1A	RO
3:0	REV	**Chip Revision Number**	0x1	RO

SPI Capabilities, SPICAP
MMS: 0
Address: 0x2
Default: 0x5A3

Bit(s)	Name	Description	Default	Access
31:11	–	Value always 0	0x0	RO
10	TXFCSVC	**TX Frame Check Sequence Verification** NCV7410 MAC supports checking the FCS on outgoing frames when not configured to compute and append the FCS to TX frames. When this feature is enabled and the MAC−PHY is operating in “store & forward” mode, frames from the SPI having an incorrect checksum are not forwarded to the line. If the MAC−PHY is operating in “cut−through” mode, incorrect frames are aborted in such a way the receiving nodes discard them.	0x1	RO
9	IPARC	**Indirect PHY Register Access** Not supported by NCV7410	0x0	RO
8	DPRAC	**Direct PHY Register Access Capability** NCV7410’s PHY registers are accessed using direct access through SPI control instructions.	0x1	RO
7	CTC	**Cut−through Capability** NCV7410 can operate in Cut−through−Mode	0x1	RO
6	FTC	**Frame Timestamp Capability** NCV7410 does not provide Frame Timestamping functionality	0x0	RO
5	AIDC	**Address Increment Disable Capability** The SPI protocol implemented into NCV7410 supports disabling the address auto−increment during control transactions, allowing the host to perform repeated read/write access to the same register.	0x1	RO
4	SEQ	**TX Data Chunk Sequence and Retry** Not supported by NCV7410	0x0	RO
3	–	Value always 0	0x0	RO
2:0	MINCPS	**Minimum Supported Chunk Payload Size** NCV7410 supports 8−byte minimum payload size. See OA−SPI specification section 9.2.3.9 for details.	0x3	RO

Reset Control and Status, RESET
MMS: 0
Address: 0x3
Default: 0x0

Bit(s)	Name	Description	Default	Access
31:1	–	Value always 0	0x0	RO
0	RESET	**Soft Reset** Writing a 1 into this bit initiated a MAC and PHY reset to their initial state. Reset starts after CS pin is de−asserted.	0	RW−SC

SPI Protocol Configuration Register, CONFIG0
MMS: 0
Address: 0x4
Default: 0x6

Bit(s)	Name	Description	Default	Access
31:16	–	Value always 0	0x0	RO
15	SYNC	**Configuration Synchronization** When set to 0, NCV7410 does not accept TX or RX frames, as its configuration may not be complete. Once the host completes the configuration of NCV7410 it should set this bit to 1. Once set, the bit can only be cleared by a system reset.	0x0	RW−1
14	TXFCSVE	**Transmit Frame Check Sequence Validation Enable** When set, the final 4 octets of all Ethernet frames conveyed via SPI are validated as an Ethernet FCS. When using this option, the FCSA bit in the MACCTRL0 shall be cleared.	0x0	RW
13	CSARFE	**CS Align Receive Frame Enable** When set, all received Ethernet frames start at the beginning of the receive chunk following the CSn assertion with a Start Word Offset of zero. When this bit is cleared, received frames may begin anywhere within the chunk payload.	0x0	RW
12	ZARFE	**Zero Align Receive Frame Enable** When set, all received Ethernet frames start at the beginning of the received chunk with a Start Word Offset of zero. When this bit is cleared, received frames may begin anywhere within the chunk payload.	0x0	RW
11:10	TXCTHRESH	**Transmit Credit Threshold** Configures the minimum number of transmit credits (TXC) that have to be available for asserting IRQn, after TXC went down to zero. 00 ≥ 1 credit (the default) 01 ≥ 4 credits 10 ≥ 8 credits 11 ≥ 16 credits	0x0	RW
9	TXCTE	**Transmit Cut Though Enable** When set to one, this bit enables sending frames in cut−through mode to reduce the average TX latency.	0x0	RW
8	RXCTE	**Receive Cut−through Enable** When set to one, this bit enables receiving frames in cut−through mode to reduce the average RX latency.	0x0	RW
7	FTSE	**Frame Timestamp Enable** This feature is not supported by NCV7410. The bit is read−only	0x0	RO
6	FTSS	**Receive Frame Timestamp Select** This feature is not supported by NCV7410. The bit is read−only	0x0	RO
5	PROTE	**Enable Control Data Read/Write Protection** Refer to OA−SPI specification section 7.4 for details	0x0	RW
4:3	–	Value always 0	0x0	RO
2:0	CPS	**Chunk Payload Size** 0x3 Chunk Payload size is 8 bytes 0x4 Chunk Payload size is 16 bytes 0x5 Chunk Payload size is 32 bytes 0x6 Chunk Payload site is 64 bytes (default)	0x6	RW

SPI Protocol Status Register, STATUS0
MMS: 0
Address: 0x8
Default: 0x40

Bit(s)	Name	Description	Default	Access
31:13	–	Value always 0	0x0	RO
12	CDPE	**Control Data Protection Error** When configured to control data read/write protection (set bit PORTE of CONFIG0 Register), this bit indicates that the MAC−PHY has detected an error in the last control transaction.	0	R/W1C
11	TXFCSE	**Transmit Frame Check Sequence Error** When set, this bit indicates that the MAC−PHY has detected that the outgoing frame's FCS added by the host is invalid. To clear this bit, write a "1" to this field.	0	R/W1C
10	TTSCAC	Always 0. Time stamping is not implemented into NCV7410	0	RO
9	TTSCAB		0	RO
8	TTSCAA		0	RO
7	PHYINT	**PHY Interrupt** When 1, the embedded PHY is generating an interrupt request. This bit can only be cleared when the interrupt event of the PHY is acknowledged. See MIIM Interrupt Control Register.	0	RO
6	RESETC	**Reset Complete** This bit is set when the reset procedure is completed and the device is ready to be configured. When set, it will generate a non−maskable interrupt on IRQn to notify the SPI host that the reset has completed. In addition, when this bit is set, the EXST bit in the RX footer is also set. To clear this bit, the host shall write a 1 to it.	1	R/W1C
5	HDRE	**Header Error** Indicates that a header error occurred since this bit was last cleared. When set, the MAC−PHY has detected an invalid header received from the SPI host due to a parity check error.	0	R/W1C
4	LOFE	**Loss of Framing Error** When 1, this bit indicates that the NCV7410 has detected a de−assertion of CS prior to the expected end of a data chunk or a command control transaction, resulting in loss of data.	0	R/W1C
3	RXBOE	**Receive Buffer Overflow Error** When 1, this bit indicates that a frame coming from the network was discarded due to the receive buffer being full.	0	R/W1C
2	TXBUE	T**ransmit Buffer Underflow Error** When 1, this bit indicates that the transmit buffer experienced an underflow condition and the transmitted frame was lost. This situation can only happen when the NCV7410 is configured to operate in TX cut−through mode.	0	R/W1C
1	TXBOE	**Transmit Buffer Overflow Error** When 1 this bit indicates that the transmit buffer overflowed and that the transmit frame data was lost.	0	R/W1C
0	TXPE	**Transmit Protocol Error** When set, this bit indicates that a TX Data Chunk error occurred. this error gets flagged under any of the following error conditions: • Data chunk with DV=1 but without a prior SV=1 • Data chunk with SV=1 but with no EV=1 (repeated SV=1). • Data Chunk indicates EV=1 without a prior SV=1 • The values of the SWO and/or EBO fields in the header exceed the CPS setting on the SPI CONFIG0 register. • (i.e. CPS set to 32bit chunk size and SWO points to bit 40) See OA−SPI protocol specification for details.	0	R/W1C

Buffer Status Register, BUFSTS
MMS: 0
Address: 0xB
Default: 0x3C00

Bit(s)	Name	Description	Default	Access
31:16	–	Value always 0	0x0	RO
15:8	TXC	**Transmit Chunks Available** The number of data chunks available in the transmit buffer. Writing chunks when TXC is 0, results in a transmit buffer overflow. The lower five bits of the TXC are also contained in the TXC field of the SPI protocol's footer (the last 4 bytes of a received data chunk). The NCV7410 provides a 4 kB buffer for TX data.	0x3C	RO
7:0	RCA	**Receive Chunks Available** The number of data chunks currently available for the SPI host to read. Reading this field allows the SPI host, for example, to queue that number of receive chunks available into a single DMA transfer. The lower 5 bits of this field are also reported in the RCA field of every RX data footer. The NCV7410 provides a 4 kB buffer for RX data.	0x0	RO

Interrupt Mask Register, IMASK
MMS: 0
Address: 0xC
Default: 0x1FBF

Bit(s)	Name	Description	Default	Access
31:13	–	Value always 0	0x0	RO
12	CDPEM	**Control Data Protection Error Mask** When set, the Control Data Protection status bit in SPI STATUS0 register does not set the EXST bit in the data footer and prevents IRQn from being asserted.	1	RW
11	TXFCSEM	**TX Frame Check Sequence Error Mask** When set, the Transmit FCS Error (TXFCSE) status bit in STATUS0 register does not set the EXST bit in the data footer and prevents IRQn from being asserted.	1	RW
10	Reserved	Value always 1	1	RO
9	Reserved	Value always 1	1	RO
8	Reserved	Value always 1	1	RO
7	PHYINTM	**PHY Interrupt Mask** When set, the physical layer interrupt (PHYINT) status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
6	RESETCM	**Reset Complete Mask** Reset Complete Mask. This bit is reserved as a mask for the Reset Complete (RESETC) status bit. This bit is read−only and always zero as the RESETC status bit is a non−maskable interrupt that will cause IRQn to always assert when RESETC is set.	0	RO
5	HDREM	**Header Error Mask** When set, a SPI Header Error (HDRE) does not assert IRQn or EXST in the data chunk footer.	1	RW
4	LOFEM	**Loss of Frame Error Mask** When set, the LOFE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
3	RXDOEM	**Receive buffer Overflow Error Mask** When set, the RXDOE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
2	TXBUEM	**Transmit Buffer Underflow Error Mask** When set, the TXBUE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
1	TXBOEM	**Transmit Buffer Overflow Error Mask** When set, the TXBOE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
0	TXPEM	**Transmit Protocol Error Mass** When set, the TXPE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW

PHY Control Register
MMS: 0
Address: 0xFF00 (65280)
Default: 0x0

Bit(s)	Name	Description	Default	Access
31:16	–	Value always 0	0x0	RO
15	RESET	**Soft Reset** 1 = PHY reset 0 = normal operation When set, a soft reset is initiated. Soft reset does not cause bootstrapping, avoiding changes in operation mode set during bootstrapping at power on or hard rest. All registers revert to their default values and any communication is interrupted. After the soft reset procedure is completed, this bit is automatically reset to 0 (its default).	0x0	RW SC
14	LOOP	**Loop−Back Mode** 1 = loopback mode enabled 0 = loopback mode disabled When set to 1, frames are looped back to the MAC rather than being sent over the line. In this mode, the transceiver is isolated from the line.	0x0	RW
13	SPD0	**Bit 0 of Speed Selection [1:0]** See Bit 6 below	0x0	RO
12	LCTL	**Link Control** 1 = PHY transmit/receive enabled 0 = PHY transmit/receive disabled Implementation is different from how it is specified in Clause 22.2.4.1.4 (Auto negotiation Enable).	0x0	RW
11	–	Value always 0	0x0	RO
10	ISOM	**Isolated Mode Enable** 1 = Isolated mode enabled 0 = Normal operation When set to 1, all pins are set to tristate except for the SPI interface and the IRQn pin. The default state depends on the bootstrap configuration.	0x0	RW
9	LRST	**Link Reset** 1 = Reset Link Status 0 = Normal Operation When set to 1, the link is reset, then normal operation resumes. This behavior differs from IEEE802.3 Clause 22.2.4.1.7, but allows the device to be managed by standard software drivers.	0x0	RW SC
8	DUPL	**Duplex Mode** 0 = Half−Duplex This is a read−only flag. A zero indicates the PHY only supports half−duplex operation.	0x0	RO
7	CTEST	**Collision Test** 1 = Collision Test enabled 0 = Normal Operation See IEEE802.3 Clause 22.2.4.1.9 for details	0x0	RW
6	SPD1	**Bit 1 of Speed Selection [1:0]** Together with bit 13 this bit indicates that the PHY only supports 10 Mb/s Both bit 6 and bit 13 always read logic zero and are read−only	0x0	RO
5:0	–	Value always 0	0x0	RO

PHY Status Register
MMS: 0
Address: 0xFF01 (65281)
Default: 0x809 (2057)

Bit(s)	Name	Description	Default	Access
31:12	–	Value always 0	0x0	RO
11	S10M	**10 Mb/s Speed Half−Duplex Mode** 1 = The PHY is a 10 Mb/s Half Duplex only device	0x1	RO
10:8	–	Value always 0	0x0	RO
7	UNIA	**Unidirectional Ability** 0 = 10BASE−T1S does not support unidirectional links	0x0	RO
6	PRSUP	**Management Preamble Suppression** 0 = The PHY does not accept MDIO frames with a suppressed preamble	0x0	RO
5	LNOK	**Link Negotiation Complete** 0 = Link negotiation in progress 1 = Link negotiation is completed The PHY sets this bit when the PHY Control register bit 12 = 1 and bit 9 = 0. This bit is further masked by PLCA status when PLCA is enabled. This prevents standard drivers from sending a packet while PLCA is starting. The implementation is different from IEEE 802.3 Clause 22.2.4.2.10 (Auto negotiation Enable), but allows the NCV7410 to be managed by standard software drivers.	0x0	RO
4	RJAB	**Remote Jabber** 0 = Remote jabber was not detected since the last read−out 1 = Remote jabber event was detected since the last read−out The fault condition is latched until this field is read or the integrated PHY is reset.	0x0	RO−LH
3	ANAB	**Auto−Negotiation Ability** 1 = The PHY does not support auto−negotiation, but the bit is set to 1 to allow the PHY to be managed by standard software drivers	0x1	RO
2	LKST	**Link Status** 0 = Valid link has not been established 1 = Valid link has been established	0x0	RO
1	LJAB	**Local Jabber** 0 = Local jabber event was not detected since the last read−out 1 = Local jabber event was detected since the last read−out The fault condition is latched until this field is read, or the integrated PHY is reset. See also 802.3cg Clause 147.3.2.9	0x0	RO−LH
0	EXTC	**Extended Capabilities** 1 = The PHY supports Clause 22 to Clause 45 bridge access mode Indicates that the integrated PHY contains registers that are in Clause 45 of the IEEE802.3 specification.	0x1	RO

PHY Identifier 0 Registers
MMS: 0
Address: 0xFF02 (65282)
Default: –

Bit(s)	Name	Description	Default	Access
31:16	–	Value always 0	0x0	RO
15:0	OUI [3:18]	**Organizational Unique Identifier [2:17]** The bit order is reversed. Bit 15 maps bit 2 of the OUI, and bit 0 maps bit 17 of the OUI. Bits 0 and 1 are 0. NOTE: **onsemi**'s OUIs can be found at: https://standards−oui.ieee.org/	–	RO

PHY Identifier 1 Registers
MMS: 0
Address: 0xFF03 (65283)
Default: –

Bit(s)	Name	Description	Default	Access
31:16	–	Value always 0	0x0	RO
15:10	OUI [19:23]	**Organizational Unique Identifier [18:23]** The bit order is reversed. Bit 15 corresponds to bit 18 of the OUI, and bit 10 corresponds to bit 23 of the OUI. NOTE: **onsemi**'s OUIs can be found at: https://standards−oui.ieee.org/	–	RO
9:4	MODEL	**IC Model Number**	0x1A	RO
3:0	REV	**Chip Revision Number**	0x1	RO

MMS1 REGISTERS

Memory Map Selection 1 contains all registers related to the Media Access Controller (MAC) of the NCV7410 device

MAC Control0 Register

MMS: 1
Address: 0x0 (0)
Default: 0x100 (256)

Bit(s)	Name	Description	Default	Access
31:22	–	Value always 0	0x0	RO
21	IPGNF	**Inter Packet Gap No Filter** 1= IPGNF enabled 0 = IPGNF disabled When enabled, the MAC does not restart the Inter Packet Gap counter if a glitch on carrier sense is detected within 2/3 of the nominal IPG period. Enabling IPGNF may help improve performance in high impulse noise environments. NOTE: This feature is non−standard and might break interoperability and degrade performance, depending on the use case. If unsure, leave IPGNF disabled.	0x0	RW
20	BKOD	**Back−Off Disable** 1= back−off disabled 0 = back−off enabled When set to one, the MAC does not perform back−off after a collision has been detected. This feature may be useful in conjunction with the PLCA RS in impulse noise environments, as it makes the MAC automatically retransmit disrupted packets. NOTE: Setting BKOD to 1 enables a non−standard feature that can affect interoperability and performance in a plain (non−PLCA) CSMA/CD network. When in doubt, leave this in the default state.	0x0	RW
19	NFCSF	**FCS Filter Disable** 1 = FCS filtering disabled 0 = FCS filtering enabled No FCS Filter: when enabled, RX frames are forwarded to the host even if their FCS (CRC) is invalid. The host can determine if an FCS error occurred by checking the FD bit in the SPI Protocol footer. See OA−SPI specification for details on the RX footer.	0x0	RW
18	MCSF	**Multicast Filter Enable** 1 = multicast filter enabled 0 = multicast filter disabled When enabled the MAC discards RX frames with a multicast destination address (first bit of the destination address set to 1). See IEEE802.3 clause 3.2.3 for details. When set, the discarded frame will be counted in the STRXDROPPED Statistics Counter (MMS 1 address 0x0052). Note that the MAC address is typically represented in little−endian bit order. The first address bit (I/G) defined in the IEEE Standard is the least significant bit of the first byte. Example: 01:54:09:AA:4C:02 is a multicast address, 84:2D:FC:65:98:07 is a unicast address	0x0	RW
17	BCSF	**Broadcast Filter Enable** 1= broadcast filter enabled 0 = broadcast filter disabled When enabled the MAC discards frames with broadcast destination address (FF:FF:FF:FF:FF:FF). If a frame is discarded as a consequence of enabling the filter, it will be counted in the STRXDROPPED statistic register (MMS1 address 0x052).	0x0	RW

(continued)

Bit(s)	Name	Description	Default	Access
16	ADRF	**Address Filter Enable** 1 = destination filter enabled 0 = destination filter disabled When enabled, the MAC checks the destination address from the incoming frame against the ADDRFILTx/ADDRMASKx compare and mask registers to decide if the frame has to be accepted or rejected. When disabled, the MAC will enter promiscuous mode, accepting every frame, regardless of its destination address. The promiscuous mode is helpful for monitoring network traffic or for implementing bridging in multi−port hosts.	0x0	RW
15:9	−	Value always 0	0x0	RO
8	FCSA	**Frame Check Sequence Append** 1 = MAC−PHY calculates & appends FCS 0 = MAC−PHY does not add FCS When enabled, the MAC inside NCV7410 computes and auto−appends the FCS (frame check sequence) to outgoing TX Frames, off−loading the host controller from having to calculate the FCS. When cleared, the MAC expects the FCS to be included in the frame data offered by the host controller. In safety−critical applications and in applications in which SPI transmission errors could occur, this feature should not be used. In such a situation the host should calculate and append the FCS prior to passing the frame data to the MAC−PHY over SPI (FCSA=0).	0x1	RW
7:2	−	Value always 0	0x0	RO
1	TXEN	**Transmit Enable** 1= TX enabled 0 = TX disabled When set, MAC transmit functions are enabled and packets conveyed by the host are forwarded to the embedded PHY. When the bit is clear, frames coming from the host interface are kept in RAM but no data is passed to the internal PHY. When TXEN is cleared during active frame transmission, the current frame will not be interrupted, but it will be fully sent to the PHY before entering the TX disable state.	0x0	RW
0	RXEN	**Receive Enable** 1 = RX enable 0 = RX disable When set, the MAC receive functions are enabled and packets from the embedded PHY are forwarded to the host. When cleared, frames coming from the PHY functions of the NCV7410 will be discarded silently and no data will be conveyed to the host. Clearing RXEN also resets all statistics registers that count RX events (MMS 1, addresser 0x0041 to 0x0052). If RXEN is cleared while a reception is ongoing, the transfer will not be interrupted. Hence, this bit can be used to perform a graceful shutdown of the MAC's RX function. If RXEN is enabled while the integrated PHY is already conveying data to the MAC, the current reception is skipped, preventing the MAC from transferring corrupted or incomplete data to the host.	0x0	RW

Address Filter 0 Low, ADDRFILT0L
MMS: 1
Address: 0x10 (16)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDFILT0 [31:0]	**Address Filter Low 0** Holds the 32 lower order bits of the Address Filter 0 that is split into ADDRFILT0L and ADDRFILT0H.	0x0	RW

Address Filter 0 High, ADDRFILT0H
MMS: 1
Address: 0x11 (17)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31	EN	**Filter 0 Enable** 1 = Filter enabled 0 = Filter disabled This bit, when set, enables the corresponding Address filter, to filter incoming frames. ADRF in the MAC Control Register (MMS 1, 0x0000 bit 16) shall be enabled for address filtering to work.	0x0	RW
30:16	–	Value always 0	0x0	RO
15:0	ADDRFILT0 [47:32]	**Address Filter 0 High** Higher order bits of the Filter Address	0x0	RW

Address Filter 1 Low, ADDRFILT1L
MMS: 1
Address: 0x12 (18)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDFILT1 [31:0]	**Address Filter 1 Low** Holds the 32 lower order bits of the Address Filter 0 that is split into ADDRFILT1L and ADDRFILT1H.	0x0	RW

Address Filter 1 High, ADDRFILT1H
MMS: 1
Address: 0x13 (19)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31	EN	**Filter 1 Enable** 1 = Filter enabled 0 = Filter disabled This bit, when set, enables the corresponding Address filter, to filter incoming frames. ADRF in the MAC Control Register (MMS 1, 0x0000 bit 16) shall be enabled for address filtering to work.	0x0	RW
30:16	–	Value always 0	0x0	RO
15:0	ADDRFILT1 [47:32]	**Address Filter 1 High** Higher order bits of the Filter Address	0x0	RW

Address Filter 2 Low, ADDRFILT2L
MMS: 1
Address: 0x14 (20)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDFILT2 [31:0]	**Address Filter 2 Low** Holds the 32 lower order bits of the Address Filter 0 that is split into ADDRFILT2L and ADDRFILT2H.	0x0	RW

Address Filter 2 High, ADDRFILT2H
MMS: 1
Address: 0x15 (21)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31	EN	**Filter 2 Enable** 1 = Filter enabled 0 = Filter disabled This bit, when set, enables the corresponding Address filter, to filter incoming frames. ADRF in the MAC Control Register (MMS 1, 0x0000 bit 16) shall be enabled for address filtering to work.	0x0	RW
30:16	–	Value always 0	0x0	RO
15:0	ADDRFILT2 [47:32]	**Address Filter 2 High** Higher order bits of the Filter Address	0x0	RW

Address Filter 3 Low, ADDRFILT3L
MMS: 1
Address: 0x16 (22)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDFILT3 [31:0]	**Address Filter 3 Low** Holds the 32 lower order bits of the Address Filter 0 that is split into ADDRFILT3L and ADDRFILT3H.	0x0	RW

Address Filter 3 High, ADDRFILT3H
MMS: 1
Address: 0x17 (23)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31	EN	**Filter 3 Enable** 1 = Filter enabled 0 = Filter disabled This bit, when set, enables the corresponding Address filter, to filter incoming frames. ADRF in the MAC Control Register (MMS 1, 0x0000 bit 16) shall be enabled for address filtering to work.	0x0	RW
30:16	–	Value always 0	0x0	RO
15:0	ADDRFILT3 [47:32]	**Address Filter 3 High** Higher order bits of the Filter Address	0x0	RW

Address Mask 0 Low, ADDRMASK0L
MMS: 1
Address: 0x20 (32)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDRMASK0 [31:0]	**Address Mask 0 Low** Holds the 32 lower−order bits of the address filter mask that is split into ADDRMASK0L and ADDRMASK0H.	0x0	RW

Address Mask 0 High, ADDRMASK0H
MMS: 1
Address: 0x21 (33)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:16	–	Value always 0	0x0	RO
15:0	ADDRMASK0 [47:0]	**Address Mask 0 High** Higher order bits of the Filter Address Mask	0x0	RW

Address Mask 1 Low, ADDRMASK1L
MMS: 1
Address: 0x22 (34)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDRMASK1 [31:0]	**Address Mask 1 Low** Holds the 32 lower−order bits of the address filter mask that is split into ADDRMASK1L and ADDRMASK1H.	0x0	RW

Address Mask 1 High, ADDRMASK1H
MMS: 1
Address: 0x23 (35)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:16	–	Value always 0	0x0	RO
15:0	ADDRMASK1 [47:0]	**Address Mask 1 High** Higher order bits of the Filter Address Mask	0x0	RW

Address Mask 2 Low, ADDRMASK2L
MMS: 1
Address: 0x24 (36)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDRMASK2 [31:0]	**Address Mask 2 Low** Holds the 32 lower−order bits of the address filter mask that is split into ADDRMASK2L and ADDRMASK2H.	0x0	RW

Address Mask 2 High, ADDRMASK0H
MMS: 1
Address: 0x25 (37)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:16	–	Value always 0	0x0	RO
15:0	ADDRMASK2 [47:0]	**Address Mask 2 High** Higher order bits of the Filter Address Mask	0x0	RW

Address Mask 3 Low, ADDRMASK3L
MMS: 1
Address: 0x26 (38)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDRMASK3 [31:0]	**Address Mask 0 Low** Holds the 32 lower−order bits of the address filter mask that is split into ADDRMASK3L and ADDRMASK3H.	0x0	RW

Address Mask 0 High, ADDRMASK3H
MMS: 1
Address: 0x27 (39)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:16	−	Value always 0	0x0	RO
15:0	ADDRMASK3 [47:0]	**Address Mask 3 High** Higher order bits of the Filter Address Mask	0x0	RW

Statistic, Sent Bytes Counter Low, STOCTETSTXL
MMS: 1
Address: 0x30 (48)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STOCTETSTXL [31:0]	**Statistic, Sent Bytes Counter Low** This register is part of the MAC statistic registers. STOCTETSXTL holds the 32 low−order bits of the cumulative sum of all data bytes sent since the register was last read. Together with the STOCTETSTXH, this register represents the number of transmitted bytes. The bytes comprise the whole frame, from the first byte of the destination address up to (and including) the frame checksum. Any padding added by the MAC is also counted. If the counter reaches its maximum value of 0xFFFFFFFFFFFF, the counter will wrap to zero. The counter clears when both STOCTETSTXL and STOCTETSTXH are being read. NOTE: Internal logic samples the high−order bits of the 48−bit byte counter into the STOCTETSTXH register, every time the STOCTETSTXL register is read. For reading the correct number of bytes transmitted, the STOCTETSTXL register must be read before reading the STOCTETSTXH register.	0x0	RO−SCR

Statistic, Sent Bytes Counter High, STOCTETSTXH
MMS: 1
Address: 0x31 (49)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:16	−	Value always 0	0x0	RO
15:0	STOCTETSTX[47:32]	**Statistic, Sent Bytes Counter High** This register is part of the MAC statistic registers. STOCTETSXTH holds the 16 high−order bits of the cumulative sum of all data bytes sent since the last read.	0x0	RO−SCR

Statistic, Frames Sent Ok, STFRAMESTXOK
MMS: 1
Address: 0x32 (50)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTXOK	**Statistic, Frames Successfully Transmitted** Holds the number of frames transmitted successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Broadcast Frames Sent Ok, STBCASTTXOK
MMS: 1
Address: 0x33 (51)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STBCASTTXOK	**Statistic, Broadcast Frames Successfully Transmitted** Holds the number of broadcast frames (destination address FF:FF:FF:FF:FF:FF) transmitted successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Multicast Frames Sent Ok, STMCASTTXOK
MMS: 1
Address: 0x34 (52)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STMCASTTXOK	**Statistic, Multicast Frames Successfully Transmitted** Holds the number of multicast frames (first bit of destination address is set to 1) transmitted successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 64−byte Frames Sent Ok, STFRAMESTX64
MMS: 1
Address: 0x35 (53)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX64	**Statistic, 64−byte frames sent ok** Holds the number of 64−byte frames transmitted successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 65−byte to 127−byte Frames Sent Ok, STFRAMESTX65
MMS: 1
Address: 0x36 (54)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX65	**Statistic, 65−byte to 127−byte Frames Sent Ok** Holds the number of frames transmitted successfully since the last read of this register, with a size between 65 bytes and 127 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 128−byte to 255−byte Frames Sent Ok, STFRAMESTX128
MMS: 1
Address: 0x37 (55)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX128	**Statistic, 128−byte to 255−byte Frames Sent Ok** Holds the number of frames transmitted successfully since the last read of this register, with a size between 128 bytes and 255 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 256−byte to 511−byte Frames Sent Ok, STFRAMESTX256
MMS: 1
Address: 0x38 (56)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX256	**Statistic, 256−byte to 511−byte Frames Sent Ok** Holds the number of frames transmitted successfully since the last read of this register, with a size between 256 bytes and 511 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 512−byte to 1023−byte Frames Sent Ok, STFRAMESTX512
MMS: 1
Address: 0x39 (57)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX512	**Statistic, 512−byte to 1023−byte Frames Sent Ok** Holds the number of frames transmitted successfully since the last read of this register, with a size between 512 bytes and 1023 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 1024−byte or More Frames Sent Ok, STFRAMESTX1024
MMS: 1
Address: 0x3A (58)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX1024	**Statistic, 1024−byte or more Frames Sent Ok** Holds the number of frames transmitted successfully since the last read of this register, with a size of 1024 bytes or more. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Aborted Frames Due to TX−buffer Underflow, STUNDERFLOW
MMS: 1
Address: 0x3B (59)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STUNDERFLOW	**Statistic, Aborted Frames Due to TX−buffer Underflow** Holds the number of frames aborted due to a TX−buffer underflow since the last read. This can only happen in cut−through mode, when the host cannot keep up sending frame data fast enough. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Frames Transmitted after a Single Collision, STSINGLECOL
MMS: 1
Address: 0x3C (60)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:18	−	Value always 0	0x0	RO
17:0	STSINGLECOL	**Statistic, Frames Transmitted after a Single Collision** Holds the number of frames transmitted after a single collision event. When PLCA is enabled, the register counts the logical collisions reported by the RS layer, rather than actual physical collisions happening on the line. In this case, a non−zero value in SINGLECOL indicates that the PLCS RS is actively arbitrating the line. It does not indicate a problem or degradation of the network performance. To read the actual number of physical collisions on a PLCA−enabled network, read the T1SPCSDIAG2 Register. The register does not overflow from its maximum value of 0x0003FFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Frames Transmitted after Multiple Collisions, STMULITCOL
MMS: 1
Address: 0x3D (61)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:18	–	Value always 0	0x0	RO
17:0	STMULTICOL	**Statistic, Frames Transmitted after Multiple Collisions** Holds the number of frames transmitted after multiple collision events. When PLCA is enabled, the register should not count any events. Multiple collisions happening on a PLCA−enabled network may indicate a misconfiguration of the fundamental parameters (e.g. TO_TIMER), the presence of non−PLCA nodes on the same medium or a defect node on the network. The register does not overflow from its maximum value of 0x0003FFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Frames Transmitted after Excessive Collisions, STEXCESSCOL
MMS: 1
Address: 0x3E (62)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	–	Value always 0	0x0	RO
9:0	STEXCESSCOL	**Statistic, Frames Transmitted after Excessive Collisions** Holds the number of outgoing frames that were aborted because of too many collisions. When PLCA is enabled, the register should not count any events. Excessive collision happening on a PLCA−enabled network may indicate misconfiguration of fundamental parameters (e.g. TO_TIMER), the presence of non−PLCA nodes on the network, or a malfunctioning node. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Frames Transmitted after Deferral, STDEFEEREDTX
MMS: 1
Address: 0x3F (63)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:18	–	Value always 0	0x0	RO
17:0	STDEFERREDTX	**Statistic, Frames Transmitted after Deferral** Holds the number of frames transmitted after being deferred. Refer to IEEE802.3 clause 5.2.2 for details. In PLCA−enabled networks, deferral is part of the arbitration mechanism; therefore, a non−zero value in this counter does not indicate a degradation of network performance. The register does not overflow from its maximum value of 0x0003FFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Counter of CRS De−assertion During Frame Transmission, STCRSERR
MMS: 1
Address: 0x40 (64)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STCRSERR	**Statistic, CRS De−assertion During Frame Transmission** Counts events, where carrier indication is de−asserted or not asserted by the PHY during transmission of a frame. A non−zero value in the register may indicate a too−high level of noise on the line. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Received Bytes Counter Low, STOCTETSRXL
MMS: 1
Address: 0x41 (65)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STOCTETSRX [31:0]	**Statistic, Received Bytes Counter Low** This register holds the 32 low−order bits of the cumulative sum of all data bytes received since the last read. Together with the STOCTETSRXH, this register represents the number of received bytes. The bytes comprise the whole frame, from the first byte of the destination address up to (and including) the frame checksum. If the counter reaches its maximum value of 0xFFFFFFFFFFFF, it will wrap to zero. The counter is cleared when both STOCTETSRXL and STOCTETSRXH are being read. NOTE: Internal logic samples the high−order bits of the 48−bit counter into the STOCTETSRXH register, every time the STOCTETSRXL register is read. For reading the correct number of bytes transmitted, the STOCTETSRXL register must be read before reading the STOCTETSRXH register.	0x0	RO−SCR

Statistic, Received Bytes Counter High, STOCTETSRXH
MMS: 1
Address: 0x42 (66)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:16	−	Value always 0	0x0	RO
15:0	STOCTETSRX [47:32]	**Statistic, Received Bytes Counter High** This register holds the 16 high−order bits of the cumulative sum of all data bytes received since the last read.	0x0	RO−SCR

Statistic, Frames Received Ok, STFRAMESRXOK
MMS: 1
Address: 0x43 (67)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRXOK	**Statistic, Frames Received Ok** Holds the number of frames received successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Broadcast Frames Received Ok, STBCASTRXOK
MMS: 1
Address: 0x44 (68)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STBCASTRXOK	**Statistic, Broadcast Frames Received Ok** Holds the number of broadcast frames (destination address FF:FF:FF:FF:FF:FF) received successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Multicast Frames Received Ok, STMCASTRXOK
MMS: 1
Address: 0x45 (69)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STMCASTRXOK	**Statistic, Multicast Frames Received Ok** Holds the number of multicast frames (first bit of destination address is set to 1) received successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 64−byte Frames Received Ok, STFRAMESRX64
MMS: 1
Address: 0x46 (70)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRX64	**Statistic, 64−byte Frames Received Ok** Holds the number of 64−byte frames received successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 65−byte to 127−byte Frames Received Ok, STFRAMESTX65
MMS: 1
Address: 0x47 (71)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRX65	**Statistic, 65−byte to 127−byte Frames Received Ok** Holds the number of frames received successfully since the last read of this register, with a size between 65 bytes and 127 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 128−byte to 255−byte Frames Received Ok, STFRAMESTX128
MMS: 1
Address: 0x48 (72)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRX128	**Statistic, 128−byte to 255−byte Frames Received Ok** Holds the number of frames received successfully since the last read of this register, with a size between 128 bytes and 255 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 256−byte to 511−byte Frames Received Ok, STFRAMESTX256
MMS: 1
Address: 0x49 (73)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRX256	**Statistic, 256−byte to 511−byte Frames Received Ok** Holds the number of frames received successfully since the last read of this register, with a size between 256 bytes and 511 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 512−byte to 1023−byte Frames Received Ok, STFRAMESTX512
MMS: 1
Address: 0x4A (74)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRX512	**Statistic, 512−byte to 1023−byte Frames Received Ok** Holds the number of frames received successfully since the last read of this register, with a size between 512 bytes and 1023 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 1024−byte or More Frames Received Ok, STFRAMESTX1024
MMS: 1
Address: 0x4B (75)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRX1024	**Statistic, 1024−byte or More Frames Received Ok** Holds the number of frames received successfully since the last read of this register, with a size of 1024bytes or more. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Dropped Too Short Frames, STRUNTERR
MMS: 1
Address: 0x4C (76)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STRUNTERR	**Statistic, Dropped Too Short Frames** Holds the number of received frames that were dropped due to their length being shorter than 64 bytes (runt frames). See Clause 4A.4.2 in the IEEE 802.3 specification. Runts are triggered by fragments resulting from collisions on CSMA/CD networks, but might also indicate poor SNR at the physical layer. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Dropped Too Long Frames STRXTOOLONG
MMS: 1
Address: 0x4D (77)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STRXTOOLONG	**Statistic, Dropped Too Long Frames** Holds the number of received frames that were dropped due to their length being longer than 1522 bytes. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Dropped FCS Error Frames STFCSERRS
MMS: 1
Address: 0x4E (78)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STFCSERRS	**Statistic, Dropped FCS Error Frames** CRC error counter. Holds the number of received frames that were dropped due to a frame check sequence mismatch. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Symbol Errors During Frame Reception, STSYMBOLERRS
MMS: 1
Address: 0x4F (79)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	–	Value always 0	0x0	RO
9:0	STSYMBOLERRS	**Statistic, Symbol Errors During Frame Reception** Holds the number of received frames that were dropped due to the PHY reporting a symbol decoding error. This may be caused by excessive differential noise on the line The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Align Errors During Frame Reception, STALIGNERRS
MMS: 1
Address: 0x50 (80)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	–	Value always 0	0x0	RO
9:0	STALIGNERRS	**Statistic, Align Errors During Frame Reception** Holds the number of received frames that were dropped because their size was not byte−aligned. This may be caused by excessive differential noise on the line or collisions when PLCA is not enabled for the network. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, RX Buffer Overflow Errors, STRXOVERFLOW
MMS: 1
Address: 0x51 (81)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	–	Value always 0	0x0	RO
9:0	STRXOVERFLOW	**Statistic, RX Buffer Overflow Errors** Holds the number of received frames that were aborted because the host failed to retrieve data at a sufficient rate to match the PHY bitrate, causing the RX buffer to overflow. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, RX Dropped Frame Count, STRXDROPPED
MMS: 1
Address: 0x52 (82)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STRXDROPPED	**Statistic, RX Dropped Frame Count** Holds the number of received frames that were successfully received but dropped because of address filtering. Dropped frames include frames that did not pass the checks against ADDRFILTx/ADDRMASKx, broadcast frames filtered by the BCSF bit setting, and multicast frames filtered by the MCSF bit setting in the MAC control Register (MMS 1, 0x0000). The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

MMS2 REGISTERS

Memory Map Selection 2 contains a direct mapping of Clause 45 MMD 3 PHY−PCS registers implemented in the NCV7410 device.

While register access through the SPI interface is always 32−bit, all MMS2 registers are 16−bit registers. The 2 most significant bytes of these registers always contain 0x0000 and cannot be altered by register writes

Devices in Package 1 Register

MMS: 2
Address: 0x5 (5)
Default: 0xB (11)

Bit(s)	Name	Description	Default	Access
15:4	−	Value always 0	0x0	RO
3	PCS	**Presence of PCS** 1 = PCS is present	0x1	RO
2	−	Value always 0	0x0	RO
1	PMA	**Presence of PMA** 1 = PMA is present	0x1	RO
0	CL22	**Presence of CL22 Registers** 1 = Indicates that the device contains Clause 22 standard registers.	0x1	RO

Devices in Package 2 Register

MMS: 2
Address: 0x6 (6)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:0	−	Value always 0	0x0	RO

10BASE−T1S PCS Control Register

MMS: 2
Address: 0x08F3 (2291)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15	PCSRST	**PCS Reset** 1 = PCS reset 0 = Normal operation Setting this bit to one sets all 10BASE−T1S PCS registers to their default state. This may change the internal state of the PHY's PCS and the state of the physical link. Setting this bit causes the PCS and the PMA PHY layers to reset.	0x0	RW−SC
14	LOOP	**Loop−Back Mode** 1 = Loopback enabled 0 = Loopback disabled When enabled, data sent by the MAC is looped back, traversing PCS TX and PCS RX. This allows testing of the 4B/5B encoder/decoder, the PCS TX/RX state machines, and the scrambler.	0x0	RW
13:0	−	Value always 0	0x0	RO

10BASE−T1S PCS Status Register

MMS: 2
Address: 0x08F4 (2292)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:8	−	Value always 0	0x0	RO
7	JAB	**PCS has Detected Local or Remote Jabber** 1 = Fault condition detected 0 = No fault condition detected When reading a one on this bit, the PCS inside the NCV7410 has detected a jabber fault condition. This can either be a local or a remote fault condition. The fault is latched until read.	0x0	RO−LH
6:0	−	Value always 0	0x0	RO

10BASE−T1S PCS Diagnostics Register 1

MMS: 2
Address: 0x08F5 (2293)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:0	REMJAB	**Remote Jabber Counter** Counts the number of detected remote jabber events since this register was last read. For details see IEEE802.3 Clause 45, MMD3 address 2293. If the count reaches 0xFFFF no more errors are counted to prevent the counter from overflowing.	0x0	RO−SC

10BASE−T1S PCS Diagnostics Register 2

MMS: 2
Address: 0x08F6 (2294)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:0	CTX	**Physical Collisions Counter** Counts the number of physical collision events detected by the PHY, since this register was last read. If the count reaches 0xFFFF no more errors are counted to prevent the counter from overflowing. NOTE: Physical collisions are caused by the superposition of signals transmitted simultaneously by more than one station on the same medium. In contrast to physical collisions, logical collisions in PLCA mode are triggered by the PCLA RS arbitration algorithm.	0x0	RO−SC

MMS3 REGISTERS

Memory Map Selection 3 contains a direct mapping of Clause 45 MMD 3 PHY−PMA registers implemented in the NCV7410 device.

While register access through the SPI interface is always 32−bit, all MMS3 registers are 16−bit registers. The 2 most significant bytes of these registers always contain 0x0000 and cannot be altered by register writes

Devices in Package 1 Register

MMS: 3
Address: 0x5 (5)
Default: 0xB (11)

Bit(s)	Name	Description	Default	Access
15:4	−	Value always 0	0x0	RO
3	PCS	**Presence of PCS** 1 = PCS is present	0x1	RO
2	−	Value always 0	0x0	RO
1	PMA	**Presence of PMA** 1 = PMA is present	0x1	RO
0	CL22	**Presence of CL22 Registers** 1 = Indicates that the device contains Clause 22 standard registers	0x1	RO

Devices in Package 2 Register

MMS: 3
Address: 0x6 (6)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:0	−	Value always 0	0x0	RO

BASE−T1 Extended Ability Register

MMS: 3
Address: 0x12 (18)
Default: 0x8 (8)

Bit(s)	Name	Description	Default	Access
15:4	−	Value always 0	0x0	RO
3	10T1S	**10BASE−T1S Capability** 1 = NCV7410 supports 10BASE−T1S	0x1	RO
2:0	−	Value always 0	0x0	RO

10BASE−T1S PMA Control Register

MMS: 3
Address: 0x08F9 (2297)
Default: 0x400 (1024)

Bit(s)	Name	Description	Default	Access
15	PMARST	**PMA Reset** Alias of Clause 22 bit 0.15 and MII Control Register bit 15 Soft Reset Setting this bit to one triggers a soft reset. The bit self−clears when the reset finishes.	0x0	RW−SC
14	TXDIS	**Transmitter Disable** 1 = Disable transmit 0 = Enable transmit When enabled, the PHY'S transmitter is shut down and TX requests from the MAC (SPI) are ignored.	0x0	RW
13:11	−	Value always 0	0x0	RO
10	MULT	**Multidrop Mode** Always 1 NCV7410 is a Multidrop device	0x1	RO
9:1	−	Value always 0	0x0	RO
0	LOOP	**PLA Loopback Mode** Same as Clause 22 bit 0.14 and MIIM Control Register MMS1, Address 0xFF00, bit 14.	0x0	RW

10BASE−T1S PMA Status Register

MMS: 3
Address: 0x08FA (2298)
Default: 0x2600 (9728)

Bit(s)	Name	Description	Default	Access
15:14	−	Value always 0	0x0	RO
13	LOOPA	**Loopback Mode** Always returns 1, indicating the PHY supports loopback	0x1	RO
12	−	Value always 0	0x0	RO
11	LPWRA	**Low−power Mode Interface** Always reads 0, the PHY does not support Low Power Mode	0x0	RO
10	MULTA	**Multidrop Mode** Always reads 1, NCV7410 supports half duplex Multidrop operation	0x1	RO
9	RFLTA	**Receive Faults Detection** Always reads 1, the PHY supports receive fault detection	0x1	RO
8:2	−	Value always 0	0x0	RO
1	RJAB	**Remote Jabber Detected** 0 = Remote jabber was not detected since the last read−out 1 = Remote jabber was detected since the last read−out Copy of Clause 22 Register 1.4 and MIIM Status Register, MMS1, Address 0xFF01, bit 4. Auto clear to zero on read. See MIIM Status register for description.	0x0	RO−LH
0	−	Value always 0	0x0	RO

10BASE−T1S Test Mode Control Register
MMS: 3
Address: 0x08FB (2299)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:13	Test Mode	**Selection of a Test Mode** 000 = Normal operation 001 = Test Mode 1 (Transmitter output voltage) 010 = Test Mode 2 (Transmitter output droop) 011 = Test Mode 3 (Transmitter PSD mask) 100 = Test Mode 4 (Transmitter High Impedance) 101 = Reserved 110 = Reserved 111 = Reserved	0x0	RW
12:0	–	Value always 0	0x0	RO

MMS4 REGISTERS

Memory Map Selection 4 contains a direct mapping of Clause 45 MMD 31 PLCA and vendor−specific PHY registers implemented in the NCV7410 device.

While register access through the SPI interface is always 32−bit, all MMS4 registers are 16−bit registers. The 2 most significant bytes of these registers always contain 0x0000 and cannot be altered by register writes

Chip Revision Register

MMS: 4
Address: 0x8000 (32768)
Default: 0x10c6 (4294)

Bit(s)	Name	Description	Default	Access
15:12	MAJ	**Major Revision** Major release number, indicating a significant change in the architecture	0x1	RO
11:8	MIN	**Minor Revision** Minor release number, indicating changes in the feature set	0x0	RO
7:6	STAGE	**Maturity Level** 00 = Alpha Test release (Incomplete set of features) 01 = Beta Test release (Full set of features) 10 = Release Candidate (release suitable for 11 = Stable (version for production)	0x3	RO
5:0	BUILD	**Build Number** Progressive number indicating a bug fix or minor feature release.	0x6	RO

PHY Configuration 1 Register

MMS: 4

Address: 0x8001 (32769)

Default: 0x3 (11)

The PHY configuration 1 register allows using non−IEEE802.3 compliant operation modes that can help with debugging and increased performance in noisy environments. Note that these settings should be used with care as they might result in a network configuration that prohibits successful communication.

Bit(s)	Name	Description	Default	Access
15	PKTLOOP	**MII Packet Loop** 1 = Packet Loop enabled 0 = Packet Loop disabled When enabled, the TX frames are reflected back to the MII RX. In contrast to PCS/PMA loopback mode (Clause 22 Register 0 bit 14), the TX packets will be transmitted to the line.	0x0	RW
14:8	–	Value always 0	0x0	RO
7	ENIE	**Enhanced Noise Immunity (ENI) Mode** 1 = Enhanced noise immunity enabled 0 = Enhanced noise immunity disabled Enhanced Noise Immunity (ENI) mode allows extending the PHY noise immunity when PLCA is enabled and active. While this is a non−IEEE standard conform feature, ENI can be used with no side effects on full PLCA−enabled networks. When all nodes on the network are PLCA configured, EMI can be further improved by masking physical collisions detection (NCOLM).	0x0	RW
6	UNJT	**UNJAB Automatic Recovery** 1 = Unjab Timer enabled 0 = Unjab Timer disabled Setting this bit enables automatic recovery from PCS TX cool down after the Unjab timer expires and the jabber condition is over. See Clause 147.3.2. of the IEEE802.3cg specification for more details.	0x0	RW
5:3	–	Value always 0	0x0	RO
2	SCRD	**PCS Scrambler Disable** 1 = PCS scrambling disabled 0 = PCS scrambling enabled When set, the PCS scrambling function is disabled and the 4B data is sent plain to the 4B/5B− and DME encoders. In addition, data received from the line is not de−scrambled after the 5B/4B conversion. This is a debug feature and is not intended to be used during normal operation.	0x0	RW
1	NCOLM	**No Collision Mode** 1 = ENI collision detection masking disabled 0 = ENI collision detection masking enabled If set, this bit prevents masking of collision detection when Enhanced Noise Immunity (ENI) mode is enabled.	0x1	RW
0	RXDLY	**MII RX Delay** 0 = MII Rx signals are not delayed 1 = MII Rx signals are delayed Setting this bit enables an additional RX path delay of 32 MII clock cycles when PLCA is enabled. NOTE: Although the default is 1, this bit can be set to 0 to decrease the RX latency by approximately 5.6 μs	0x1	RW

PLCA Extensions Register
MMS: 4
Address: 0x8002 (32770)
Default: 0x800 (2048)

Bit(s)	Name	Description	Default	Access
15	PREN	**PLCA Precedence Mode** 1 = Precedence Mode enabled 0 = Precedence Mode disabled While in Precedence Mode, the PLCA Reconciliation Layer implicitly terminates a cycle at each transmitted or received packet, causing the network to behave more like a CAN network where nodes with lower local node IDs get strict precedence over nodes with higher PLCA IDs.	0x0	RW
14:12	–	Value always 0	0x0	RO
11	MIIDIS	Although not being read−only, this bit is reserved and should always be kept at 1.	0x1	RW
10:2	–	Value always 0	0x0	RO
1	LDEN	**Coordinator Selection Enable** 0 = PLCA Coordinator is selected by PLCA ID (ID 0 = coordinator) 1 = PLCA Coordinator is selected by LDR bit When enabled the NCV7410 Leader role is determined by the Leader bit setting in this register. When disabled the NCV7410 takes the PLCA leader role if its PLCA ID is set to 0 in the PLCA Control 1 register.	0x0	RW
0	LDR	**Coordinator Selection** 1 = PHY is PLCA coordinator 0 = PHY is PLCA follower When the Coordinator selection enable bit in this register is set to 1 and this bit is also set to 1 the PHY operates in PLCA coordinator mode, when PLCA mode is enabled in PLCA Control 0 register.	0x0	RW

PMA Tune 0 Register

MMS: 4

Address: 0x8003 (32771)

Default: 0x2005 (8197)

This register allows fine−tuning of the NCV7410 line receiver.

WARNING: Changing the setting from their default should only be considered by experienced users at their own risk. Invalid settings may lead to unexpected link down and dropped or corrupted Ethernet frames.

Bit(s)	Name	Description	Default	Access
15:14	–	Value always 0	0x0	RO
13:8	BDT	**PLCA Beacon Detection Threshold** This field selects the threshold level for the PLCA Beacon (NN*) detection in the PMA. Higher numbers reduce the chance of false detection (false positive) bit reduces the noise tolerance. Lower numbers achieve the opposite effect.	0x20	RW
7:3	–	Value always 0	0x0	RO
2:0	DCWS	**Drift Compensation Window Selection** Selects the size of the integration window for the clock drift compensator inside the RX PMA. A lower value allows for compensation of more drift at the expense of jitter rejection. Higher values achieve the opposite effect.	0x5	RW

Window Selection Value	Integration Window Size
0	7−bit times
1	15−bit times
2	31−bit times
3	63−bit times
4	127−bit times
5	155−bit times
6	210−bit times
7	255−bit times

PMA Tune 1 Register

MMS: 4

Address: 0x8004 (32772)

Default: 0x3520 (13600)

This register allows fine−tuning of the NCV7410 line receiver.

WARNING: Changing the setting from their default should only be considered by experienced users at their own risk. Invalid settings may lead to unexpected link down and dropped or corrupted Ethernet frames.

Bit(s)	Name	Description	Default	Access
15:14	–	Value always 0	0x0	RO
13:8	PPDT	**Packet Preamble Detection Threshold** Sets the threshold level for the packet preamble (JJHH) detection in the PMA. Higher numbers reduce the chance of false detection (false positive) bit reduces the noise tolerance. Lower numbers achieve the opposite effect.	0x35	RW
7:6	–	Value always 0	0x0	RO
5:0	CDT	**Commit Detection Threshold** Sets the threshold for the Commit (JJ) detection of the PMA. Higher numbers reduce the chance of false detection (false positive) bit reduces the noise tolerance. Lower numbers achieve the opposite effect.	0x20	RW

PLCA Register Map and Identification Register, PLCIDVER

MMS: 4
Address: 0xCA00 (51712)
Default: 0x0A10 (2576)

Bit(s)	Name	Description	Default	Access
15:8	MAPID	**The Memory Map Identifier** Indicates compatibility with the OA PLCA memory map definition	0x0A	RO
7:0	MAPVER	**The Memory Map Version** Indicated the version of the OA memory map definition, the memory map in the NCV7410 device adheres to	0x10	RO

PCLA Control 0 Register, PLCACTRL0

MMS: 4
Address: 0xCA01 (51713)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15	EN	**PLCA Enable** 1 = PCLA enabled 0 = PCLA disabled When enabled the PCLA RS functions are switched on. Otherwise, the PHY behaves in CSMA/CD half−duplex mode.	0x0	RW
14	RST	**PLCA Reset** 1 = PLCA reset 0 = normal operation When set the PLCA RS is reset to its initial state. NCV7410 registers are not altered by this reset. Upon PCLA reset, the bit is auto−cleared.	0x0	RW−SC
13:0	−	Value always 0	0x0	RO

PCLA Control 1 Register, PLCACTRL1

MMS: 4
Address: 0xCA02 (51714)
Default: 0x08FF (2303)

Bit(s)	Name	Description	Default	Access
15:8	NCNT	**Node Count** Configures the number of transmit opportunities generated in a PLCA cycle. This parameter is only meaningful when the PLCA Local Node ID is set to 0x0, indicating that the PHY is operating as a coordinator node in a PLCA−enabled network.	0x08	RW
7:0	ID	**PLCA Node ID** Set the PHY's node ID in a PLCA−enabled network. This number shall be less than the Node count (see bits 15:8) set for the PLCA coordinator node. When set to 0x0 the PHY acts as the PLCA coordinator.	0xFF	RW

PCLA Status Register, PLCASTATUS

MMS: 4
Address: 0xCA03 (51715)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15	PST	**PLCA Status** When one, this bit indicates that the PLCA RS is receiving / transmitting the Beacon. Note that only the node with the ID set to 0x00 transmits the Beacon (or the one set to coordinator role using bit 1 and bit 0 of the PLCA extensions register at MMS4, address 0x8002). When the bit reads as 0, then the PHY is not ready to send or receive data in PLCA mode. This could also interpreted as an indicator of PLCA activity on the line.	0x0	RO
14:0	–	Value always 0	0x0	RO

PCLA Transmit Opportunity Timer Register, PLCATOTMR

MMS: 4
Address: 0xCA04 (51716)
Default: 0x18 (24)

Bit(s)	Name	Description	Default	Access
15:8	–	Value always 0	0x00	RO
7:0	TOTMR	**Transmit Opportunity Timer** Defines the minimum duration, in bit time, of the PLCA transmit opportunity timer as described in the OA PLCA register specification. The default value is 24BT (2.4 μs). Larger values allow for extending the maximum reach of the mixing segment, while lower values improve performance by reducing the overall unused TO time. See IEEE802.3cg Claus 30 and Claus 148 for a details description. This parameter needs to be set to the same value across all nodes sharing the same media. NOTE: According to OPEN Alliance, the default value should be 32BT (3.2 μs) = 0x20	0x18	RW

PCLA Burst Mode Register, PLCABURST

MMS: 4
Address: 0xCA05 (51717)
Default: 0x80 (128)

Bit(s)	Name	Description	Default	Access
15:8	MAXBC	**Maximal Burst Count** Sets the number of **additional** Ethernet frames that may be transmitted during a single transmit opportunity. The default allows only one frame to be sent per transmit opportunity. See IEEE802.3cg Clause 148.4.4.2 for more details.	0x0	RW
7:0	BTMR	**Burst Timer** Sets the number of bit times that PLCA RS waits for the MAC to send a frame after CRS is de−asserted. The default of 128 considers the minimum inter−frame gap of 96 bits, as defined in IEEE802.3 Clause 4.4.2, plus additional margin. Can be used to accommodate non−standard MACs that use a different length for IFG or to fine−tune performance.	0x80	RW

MMS12 REGISTERS

Memory Map Selection 12 contains a direct mapping of Clause 45 MMD 30 vendor−specific registers implemented in the NCV7410 device.

While register access through the SPI interface is always 32−bit, all MMS12 registers are 16−bit registers. The 2 most significant bytes of these registers always contain 0x0000 and cannot be altered by register writes

MIIM Interrupt Control Register

MMS: 12
Address: 0x0010 (16)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:6	−	Value always 0	0x0	RO
5	MIPCE	**Physical Collision MIIM Interrupt Enable** 1 = PHYINT on Physical Collision enabled 0 = PHYINT on Physical Collision disabled If enabled, a PHYINT is issued every time a physical collision is detected.	0x0	RW
4	MIPRE	**PLCA Recovery MIIM Interrupt Enable** 1 = PHYINT on PLCA Recovery enabled 0 = PHYINT on PLCA Recovery disabled When enabled, a PHYINT is issued on every PLCA Recovery event. PCLA recovery is flagged when a false carrier event (i.e. impulse noise) occurs on the line. When a CRS event is not followed by the reception of a packet within in certain amount of time the PHY goes to either of two states, depending on its PLCA settings: When configured as PLCA coordinator, the PHY waits for the line to be quiet for a certain amount of time and then sends a new beacon. When configured as a follower, the PHY will wait for a Beacon before getting a new transmit opportunity.	0x0	RW
3	MIRJE	**Remote Jabber MIIM Interrupt Enable** 1 = PHYINT on Remote Jabber enabled 0 = PHYINT on Remote Jabber disabled When enabled, a PHYINT is issued every time the PHY detects a remote jabber condition. A remote jabber condition exists if a station transmits for longer than a maximum length Ethernet frame transmit duration (1518 bytes, not counting Preamble and inter−packet gap).	0x0	RW
2	MILJE	**Local Jabber MIIM Interrupt Enable** 1 = PHYINT on Local Jabber enabled 0 = PHYINT on Local Jabber disabled When enabled, a PHYINT is asserted when the PHY detects a local jabber condition.	0x0	RW
1	MIPSE	**PLCA Status MIIM Interrupt Enable** 1 = PHYINT on change of PLCA Status enabled 0 = PHYINT on change of PLCA Status disabled When enabled, the device issues a PHYINT every time the PLCA Status changes. To determine the actual PLCA status the host interrupt service routine would have the read the PCLA Status Register, PLCASTATUS at MMS 4, Address 51715 (0xCA03).	0x0	RW
0	MILSE	**Link Status MIIM Interrupt Enable** 1 = PHYINT on change of Link Status enabled 0 = PHYINT on change of Link Status disabled When enabled, a PHYINT is issued every time the Link status changes. The actual link status can be read from the Link Status bit (0.2) in the PHY Status Register MMS 0, Address 0xFF01,	0x0	RW

MIIM Interrupt Status Register

MMS: 12

Address: 0x0011 (17)

Default: 0x8000 (32768)

Whenever a PHYINT occurs, the user should read this register to determine the source of the interrupt. All the bits latch high and self−clear on the read of this register.

Bit(s)	Name	Description	Default	Access
15	RSTS	**Reset** This bit is set at Power On Reset or any other form of hardware reset. Its purpose is to notify the host of a possibly unsolicited system reset. When set, it does not generate an interrupt. Once cleared it cannot be set. The bit can be cleared by writing a “1” to it.	0x1	R/W1C
14:6	–	Value always 0	0x0	RO
5	MIPCL	**Physical Collision MIIM Interrupt** Indicates that the last PHYINT was issued due to a Physical collision on the line.	0x0	R−LH
4	MIPRL	**PLCA Recovery MIIM Interrupt** Indicates that the last PHYINT was issued by the PHY due to a PLCA Recovery condition.	0x0	R−LH
3	MIRJL	**Remote Jabber MIIM Interrupt** Indicates that the last PHYINT was issued by the PHY due to detecting a remote jabber fault.	0x0	R−LH
2	MILJL	**Local Jabber MIIM Interrupt** A one indicates that the last PHYINT was issued by the PHY due to detecting a remote jabber fault.	0x0	R−LH
1	MIPSL	**PLCA Status MIIM Interrupt** Indicates that the last PHYINT was issued due to a change in PLCA status. To determine the actual PLCA status the host interrupt service routine would have the read the PCLA Status Register, PLCASTATUS at MMS 4, Address 51715 (0xCA03).	0x0	R−LH
0	MILSL	**Link Status MIIM Interrupt** Indicates that the last PHYINT was issued due to a change in the Link Status. The actual link status can be read from the Link Status bit (0.2) in the PHY Status Register MMS 0, Address 0xFF01.	0x0	R−LH

DIO Configuration Register

MMS: 12

Address: 0x0012 (18)

Default: 0x6060 (24672)

The DIO configuration register sets the function of the General Purpose I/O pins DIO1 and DIO0.

Bit(s)	Name	Description	Default	Access
15	SLR1	**DIO1 – Slew Rate** 1 = slow 0 = fast	0x0	RW
14	PEN1	**DIO1 – Pull−up/Pull−down Enable** 1= enabled 0 = disabled	0x1	RW
13	PUD1	**DIO1 – Pull−up/Pull−down Selector** 1 = Pull Down 0 = Pull Up Sets the type of the internal pull, when bit 14 is enabled	0x1	RW
12:9	FN1	**DIO1 – Function Selector** Select the function of the DIO1 pin. See Table 10 below.	0x0	RW
8	VAL1	**DIO1 – Output Value** Sets the output value of DIO1 when FN1[3:0] configure DIO1 for GPIO function It sets the polarity (1 = active high, 0 = active low) for all other modes	0x0	RW
7	SLR0	**DIO0 – Slew Rate** 1 = slow 0 = fast	0x0	RW
6	PEN0	**DIO0 – Pull−up/Pull−down Enable** 1= enabled 0 = disabled	0x1	RW
5	PUD0	**DIO0 – Pull−up/Pull−down Selector** 1 = Pull Down 0 = Pull Up Sets the type of the internal pull, when 6 is enabled	0x1	RW
4:.1	FN0	**DIO0 – Function Selector** Select the function of the DIO1 pin. See Table 10 below.	0x0	RW
0	VAL0	**DIO0 – Output Value** Sets the output value of DIO0 when FN0[3:0] configure DIO0 for GPIO function It sets the polarity (1 = active high, 0 = active low) for all other modes	0x0	RW

Table 10. DIOX FUNCTION SELECTOR DESCRIPTION

FNx[3:0]	Function	Description
0x0	Disable	DIOx is put in tristate (default)
0x1	GPIO	DIOx state corresponds to VALx
0x2	SFD−TX	Generates a pulse at SFD transmission. VALx sets the pulse polarity
0x3	SFD−RX	Generates a pulse when SFD is detected during the read. VALx sets the pulse polarity
0x4	LED − Link Control	Pin drives an LED when link is enabled and link status is up
0x5	LED − PLCA Status	Pin drives an LED when PLCA status is up
0x6	LED TX	LED indicating TX activity
0x7	LED RX	LED indicating RX activity
0x8	CLK25M	Output 25 MHz clock
0x9 − 0xA	Reserved	Don't use
0xB	SFD − RX&TX	Pulse on DIOx at SDF (RX or TX), VALx sets the polarity of the pulse
0xF	LED − TX&RX	LED indicating TX and RX activity

Topology Discovery Control Register
MMS: 12
Address: 0x0016 (22)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15	TD_ED	**Topology Discovery Enable** 1 = Enable Topology Discovery functions 0 = Disable Topology Discovery functions When enabled, the device operates in Topology Discovery mode. Data transmission is disabled while in Topology Discovery mode. Note that network communication is not possible, while a topology discovery measurement or calibration is ongoing.	0x0	RW
14:11	–	Value always 0	0x0	RO
10	CALM	**TopDisc Calibration/Measurement Selector** 1 = Calibration 0 = Measurement This bit selects the functions that should be executed when STRT is set to one, while the device is set to manual Topology Discovery mode (MANM = 1). When in automatic mode (MANM = 0) this bit has no effect on the Topology Discovery measurement sequence (automatic calibration and measurement).	0x0	RW
9	MANM	**TopDisc Manual/Automatic Mode Selector** 1 = Manual Mode 0 = Automatic Mode When this bit is set, the Topology Discovery is set to manual mode. In this mode, the user needs to manually (by means of setting the CALM bit) trigger either calibration or measurement functions. A measurement always needs to be preceded by a calibration run.	0x0	RW
8	STRT	**TopDisc Start** 1 = Start 0 = wait (default) Writing a 1 into this bit and while in Manual mode, the function selected by CALM will be started. In Automatic mode, both calibration and measurement will be performed.	0x0	RW−SC
7:5	–	Value always 0	0x0	RO
4	SCRDIR	**Scrambler Check Disable** 0: check scrambler during measurement 1: do not check the scrambler during the measurement	0x0	RW
3:1	–	Value always 0	0x0	RO
0	REFN	**TopDisc Reference/Measured Mode Selector** 1 = Reference node 0 = Measured node Sets the role of the device for Topology discovery. When in reference mode, the device initiates the transmission of measurement pulses. A device configured in measured mode returns pulses that it receives, but never actively starts a pulse transmission without prior reception of a pulse on the line coming from the reference node.	0x0	RW

Topology Discovery Status Register
MMS: 12
Address: 0x0017 (23)
Default: 0x8000 (32768)

Bit(s)	Name	Description	Default	Access
15	DONE	**TopDisc Done** When this bit contains a one, the function requested to be performed by the combination of CLAM and MAN (calibration, measurement, or automatic sequence) has finished and the results can be read from the Topology Discovery Result register. Note that there is no valid data stored for the user after a manual calibration. When automatic mode or manual measurement is performed, the user should evaluate the content of the result register.	0x1	RO
14:3	–	Value always 0	0x0	RO
2	HNDE	**TopDisc Handshake Error** When done is set to one and the last topology discovery command was run in automatic mode, a one in this bit will indicate that a handshake error has occurred and the measurement is invalid.	0x0	RO
1	MEAE	**TopDisc Measure Error** 0 = no measurement error during the last executed measurement procedure 1 = error occurred during the last measurement procedure When DONE = 1, this bit indicates that a performed measurement (both, manual and automatic mode) ended with an error. This is an indication that the measurement result stored in the result register is invalid and should be discarded. Instead, the measurement needs to be re−run. This can also be an indication of a connection issue between the two Topology discovery partners (broken cable, short, wrong termination).	0x0	RO
0	CALE	**TopDisc Calibration Error** When DONE = 1, this bit indicates that there was an error during the calibration and the device could not find a calibration solution. This can point to a defective device or traffic on the cable, caused by a network station unaware of a Topology discovery procedure on the cable. The user shall arrange that no other station, than the two stations involved in the Topology discovery, occupies the medium. Calibration errors will be flagged regardless of the operating mode (manual or automatic Topology discovery).	0x0	RO

Topology Discovery Result Register
MMS: 12
Address: 0x0018 (24)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:0	CNTV	**Topology Discovery Measurement Result** When the DONE flag in the Status register is set to 1, this register holds the number of pulses counted during the last measurement.	0x0	RO

Topology Discovery Precision Register
MMS: 12
Address: 0x0019 (25)
Default: 0x0FA0 (4000)

Bit(s)	Name	Description	Default	Access
15:0	RTMP	**Topology Discovery Precision Time** Indicates the reference counter precision in 10ps units. The value is implementation implementation−dependent and fixed to 40ns for NCV7410.	0x0FA0	RO

Topology Reference Counter Timer Register
MMS: 12
Address: 0x001A (26)
Default: 0x7530 (30000)

Bit(s)	Name	Description	Default	Access
15:0	RCNT	**TopDisc Measurement Duration** This register sets the duration of the measurement in 40 ns (RMPT of register MMS12 0x0019) increments. The default value of 20000 sets the Topology measurement duration to 0.8 ms, yielding an error of less than 4cm in precision on a 25m long cable at a propagation delay of 5ns/m.	0x7530	RW

NOTE: For calculating distance with the use of the topology discovery measurement use the following equation:

$$\text{Distance} = \frac{4 \times \text{RCNT}}{\text{CNTV}} - 16 \quad \text{(Assume a propagation delay on the cable of 5 ns/m)}$$

Example: With RCNT, set to 20000 a measurement was performed and yielded in a CNTV value of 3076:

$$\text{Distance} = \frac{4 \times 20000}{3076} - 16 = 10 \text{ m}$$

PHY Configuration 0 Register

MMS: 12

Address: 0x1001 (4097)

Default: 0x2ca1 (11425)

The PHY Configuration 0 register allows experienced users to customize the parameters of the Analog line driver among other custom parameters. The default values have been carefully selected and would not need modification under normal conditions.

Bit(s)	Name	Description	Default	Access
15:14	TX_GAIN	**Transmitter Output Amplitude** 0 = 1 Vpp 1 = 1.1 Vpp 2 = 0.9 Vpp 3 = 0.8 Vpp	0x0	RW
13:10	RX_CD	**Receiver Collision Detection Threshold** RX_CD threshold [mVpp] = 150 + (RX_CD x 50) (default = 700 mVpp) NOTE: Setting a small threshold level improves noise immunity but may increase the chance of mis−detecting a collision.	0xB	RW
9:6	RX_ED	**Received Energy Detection Threshold** RX_ED threshold [mVpp] = 150 + (RX_ED x 50) (default = 250 mVpp) NOTE: Threshold shall be set high enough to reject the noise and low enough to detect the worst−case signal amplitude on the line.	0x2	RW
5	DSLEW	**Digital Output Driver Slew Rate** Sets slew rate of all digital output pins 0 = Slow 1 = Fast	0x1	RW
4:3	CMC	**Common Mode Choke Resistance Compensation** This field should be set according to the resistance of the used CMC 00 = 0 − 0.5 Ω 01 = 0.5 − 2.25 Ω 10 = 2.25 − 3.75 Ω 11 = 3.75 − 5 Ω	0x0	RW
2	TXSLEW	**Transmitter Slew Rate** 0 = Slow 1 = Fast	0x0	RW
1	−	Value always 0	0	RO
0	CLKO_EN	**25 MHz Clock Output Enable** 0 = 25 MHz clock is not enabled to be output on CLK_O pin 1 = 25 MHz clock is enabled to be output on CLK_O pin	0x1	RW

MACID0

MMS: 12

Address: 0x1002 (4098)

Default: −

Bit(s)	Name	Description	Default	Access
15:0	MACID [15:0]	Lower 16 bits of the unique MAC address. Together with the upper 8 bits in the MACID1 register, and the OUI from IDVER (MMS0, address 0x0000, bits 31:10), it forms a unique MAC address for the NCV7410 device. Note that no Address Filter is pre−initialized with that MAC address. The user should read MACID0, MACID1, and OUI (from IDVER) to initialize the address filters. The host may also need to use the MAC address as the source address in Ethernet frames sent to the NCV7410.	−	RO

MACID1
MMS: 12
Address: 0x1003 (4099)
Default: –

Bit(s)	Name	Description	Default	Access
15:8	–	Value always 0	0x0	RO
7:0	MACID[23:16]	Upper 8 bits of the MAC address see the description in MACID0 for details.	–	RO

Chip Info Register
MMS: 12
Address: 0x1004 (4100)
Default: –

Bit(s)	Name	Description	Default	Access
15	–	Value always 0	0x0	RO
14:8	Wafer_Y	Y position on the Wafer where the part was picked from	N/A	RO
7	–	Value always 0	0x0	RO
6:0	Wafer_X	X position on the Wafer where the part was picked from	N/A	RO

NVM Health Register

MMS: 12

Address: 0x1005 (4101)

Default: 0x0

This register reports if there are errors in the trim and configuration data set by **onsemi** during manufacturing of the NCV7410.

There are three different zones for the trim & configuration data stored inside the device's nonvolatile configuration memory:

Zone	Description
Green	Manufacturing related data Errors in this zone do not cause any failure or misbehavior in the application.
Yellow	Functional Data: MAC and OUI Corrupted data in this area does not cause the part to malfunction, but a host relying on the information stored here might not initialize its drivers correctly. However, countermeasures taken in the host's software could be used to fall back to a state where operation is still possible.
Red	Trim data Data corruption in this area will render the part unusable. With trimming not being correct, it cannot be guaranteed that the part will operate within the limits required by IEEE802.3cg.

Note that the configuration & trim memory cannot be written by the user, so corrupted data cannot be recovered.

The trim & configuration memory is protected by an ECC scheme that allows the correction of single−bit errors and the detection of double−bit errors. With this, a single−bit error (SBERR) can be considered a warning, while a reported double−bit error needs to be interpreted as an error impairing the function of the part partially or entirely, depending on the zone in which it appears.

Bit(s)	Name	Description	Default	Access
15	Red Zone NVM Warning	When this bit reads as one, the ECC controller for the trim and configuration memory has detected a single−bit error in the red zone. As single−bit errors are corrected by the ECC controller, this is a warning only. NCV7410 remains fully functional.	0	RO
14	Red Zone NVM Error	When one, the ECC controller detected a 2−bit error on the trim and configuration memory that is not correctable. This needs to be treated as an error and correct functionality is not guaranteed anymore. The part might still operate with degraded performance.	0	RO
13	Yellow Zone NVM Warning	When one, the ECC controller detected and corrected a single−bit error in the yellow zone of the trim and configuration memory. Full functionality is still given.	0	RO
12	Yellow Zone NVM Error	When one, the ECC controller detected a 2−bit error in the yellow zone of the trim and configuration memory, which it cannot correct. While this is an error invalidating the content of the OUI and the MAC ID, NCV7410 will still function as an Ethernet PHY in accordance to IEEE802.3cg.	0	RO
11	Green Zone NVM Warning	When one, the ECC controller detected and corrected a single−bit error in the green zone of the trim and configuration memory. Full functionality is still given.	0	RO
10	Green Zone NVM Error	When one, the ECC controller detected a 2−bit error in the yellow zone of the trim and configuration memory, which it cannot correct. As the green zone contains manufacturing and tracing information, NCV7410's functionality is not impacted. However, the part with this error loses its manufacturing traceability.	0	RO
9:0	Reserved	Reserved for manufacturing purposes	−	RO

APPLICATIONS INFORMATION

Clock Source

The NCV7410 requires a precise and robust 25 MHz clock source for correct operation.

The clock can either be fed from an external 25 MHz clock source or be generated using a quartz crystal connected to the XTAL Oscillator circuit of the NCV7410.

Crystal Oscillator

The oscillator circuit is designed to drive a 25MHz parallel resonance AT cut quartz crystal. The external crystal shall be connected between the XI pin and the XO pin. XI is the input pin and XO is the output pin of the internal crystal oscillator circuit.

A typical crystal connection circuit is shown in Figure 5.

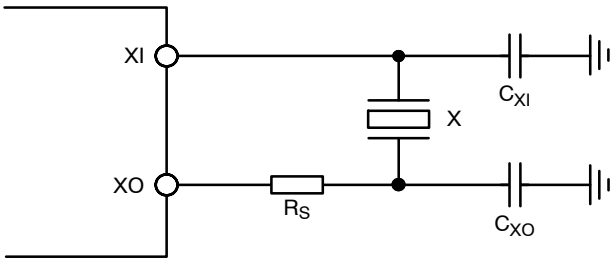


Figure 5. Crystal Connection Diagram

External Clock Source

In situations where a 25 MHz (±100 ppm) clock signal is already available in the system that utilizes the NCV7410 can be clocked using such a signal, removing the need of additional crystal and load capacitors. In this case, the external clock signal is connected to the XI pin of the NCV7410, while the XO pin shall be left floating.

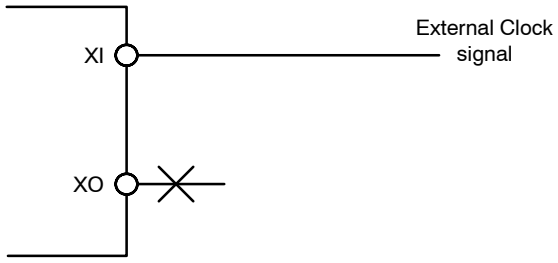


Figure 6. Connecting an External Clock Source

Clock Output

The NCV7410 also offers a dedicated output pin that can provide a stable 25 MHz clock to other components (like MCUs) on the same PCB. The CLK_O pin offers that function at 3.3 V or 2.5 V LVCMOS levels depending on the VDDIO.

DEVICE CONFIGURATION EXAMPLES

To configure the NCV7410, configuration registers (see memory map) can be set using the SPI command following the Open Alliance TC6 10BASE−T1S serial communication protocol.

Please see the “OPEN Alliance 10BASE−T1x MAC−PHY Serial Interface” specification section 7.4, available at https://www.opensig.com, for details.

Basic Configuration for CSMA/CD Operation

To connect the NCV7410 device to 10BASE−T1S multidrop network in CSMA/CD operation it needs a series of register write commands that set dedicated configuration bits in the configuration registers. Operation requires configuring the MAC and the PHY functions inside the device and finally setting the SPI to enable the exchange of Ethernet frames between the MAC−PHY and the connected SPI master (host MCU).

For CSMA/CD mode, follow the procedure shown below.

1. Issue a device reset by setting bit writing 0x00000001 into Reset Control and Status, RESET
2. In the MAC CONFIG0 register at MMS1, Address 0x0000, the following bits:
   - Bit 8: configures the MAC to calculate and append the FCS, off−loading the host from having to compute and send the FCS
   - Bit 1: enable TX functionality, allowing the MAC to send Ethernet frames to the PCS
   - Bit0: enable RX functionality, allowing the MAC to receive Ethernet frames from the PCS

   Please refer to the register description of the MAC Config0 register for more options, as the above setting represents the minimum required setting.

   The MAC is now configured to operate in “promiscuous”−mode, accepting all valid Ethernet frames, regardless of their destination address.
3. Enable the physical link by setting bit 12 of the “PHY Control Register” at MMS0, Address 0xFF00
4. Configure the SPI protocol engine according to the application needs, by setting the appropriate bits in the SPI Config0 Register at MMS0, address 0x0004.

   NOTE: A good starting point is writing 0x0000BC06 but is dependent on the implementation and capabilities of the software running on the host.

- Note that at least the SYNC bit needs to be set to one to allow data to flow between the host and the MAC−PHY.

The above four steps set the NCV7410 in CSMA/CD mode, accepting all valid Ethernet frames (“promiscuous” mode). This mode is useful when implementing traffic monitors, bridges, or interface converters.

Basic Configuration for PLCA Operation

The NCV7410 offers an optional, IEEE802.3cg specified, feature of Physical Layer Collision Avoidance.

When set to PLCA, the coordinator (typically PLCA ID 0) starts a PLCA cycle by putting a beacon on the line that is seen and recognized by all stations configured to operate in PLCA mode. PLCA only works properly, when all stations on the shared multidrop segment have a valid PLCA configuration. Requirements are:

- Every station needs to have a unique PLCA ID in the range of 0 to 255
- There is exactly one coordinator.
- The coordinator needs to have configured a PLCA node count, which needs to be greater than the highest ID assigned to the stations in the mixing segment.

In addition to the basic setup for CSMA/CD, users need to set the coordinator:

1. The local PLCA ID to 0 and the appropriate PLCA node count to allow all stations to participate in the PLCA−enabled segment − This is done by setting the correct numbers on the PLCACTRL1 register at MMS4, Address 0xCA02
2. Enable the PLCA by writing a one to PLCACTRL0 (MMS4, Address 0xCA01) at bit 15

For all other nodes in the PLCA−enabled network, the local PLCA ID shall be unique, but there is no need to specify the PLCA node count. This can be left at default or can be set to any other valid number. PLCA shall be enabled as well by writing a one to PLCACTRL0 at bit 15.

Address Filtering

Running the NCV7410 in promiscuous mode will generate a lot of traffic on the SPI interface. This might not be desired in stations limited in performance (like low−cost/low−power MCUs) that could not cope with constant traffic of 10 Mbit/s.

In a typical application, it is desired to have the MAC−PHY only forward Ethernet frames that match certain destination MAC addresses.

The NCV7410 offers a flexible scheme of up to four address match registers and filter masks allowing it to forward only the frames that match dedicated destination addresses or groups of destination addresses.

These could be Broadcasts, Multicast, and Unicast addresses.

To accept broadcast frames, the MAC Control0 register (MMS1, address 0x0000) needs to set its ADRF and clear its BCSF.

To allow the MAC−PHY to forward multicast packages to the host, set the ADRF and clear the MCSF bits in the MAC Control0 register.

In the canonical case of a station being assigned a dedicated MAC address that it should respond to the ADDRFLTH, ADDRFLTL, ADDRMASKL and ADDRMASKH registers have to be set accordingly.

These filters can also be used to limit the multicast frames to dedicated multicast IDs or a larger group of IDs or unicast addresses.

Example A:

The NCV7410 should be set to forward all Broadcast frames and frames with the destination address 60:C0:BF:01:01:01

Solution:

- Set ADDRFLT0L to 0xBF010101
- Set ADDRFLT0H to 0x800060C0
  Note that bit 31 of ADDRFLTxH activates that filter
- Set ADDRMSK0L to 0xFFFFFFFF
- Set ADDRMSK0H to 0x0000FFFF
- Set bit ADRF and clear bit BCSF in the MAC Controll0 register to one.

Example B:

In addition to Example A, the MAC−PHY should also listen forward all multicast frames of the group 31:6E:17:XX:XX:XX

Solution:

ADDRFLT1L = 0x17000000
ADDRFLT1H = 0x8000316E
ADDRMASK1L = 0xFF000000
ADDRMASK1H = 0x0000FFFF

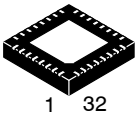
ORDERING INFORMATION

Device Order Number	Marking	Package Type	Shipping†
NCV7410MWR2G	V7410	QFNW32 (Pb−Free)	5000 / Tape & Reel

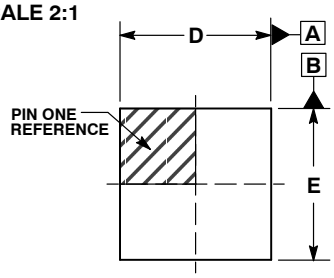
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

QFNW32 5x5, 0.5P
CASE 484AB
ISSUE D

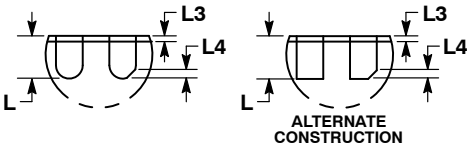
DATE 07 SEP 2018



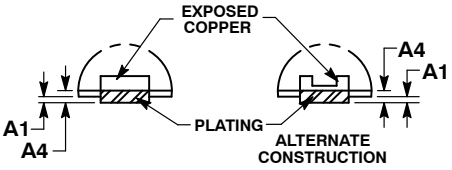
SCALE 2:1



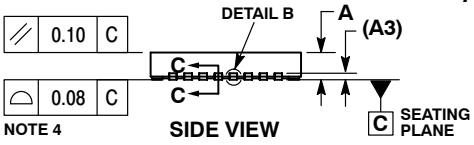
TOP VIEW



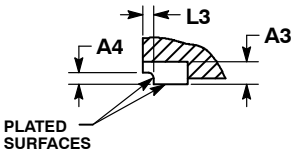
DETAIL A



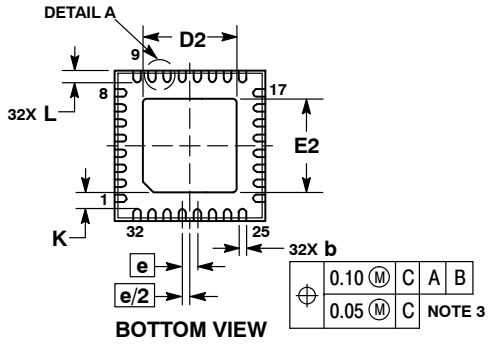
DETAIL B



SIDE VIEW



SECTION C–C

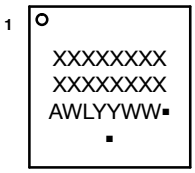


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	---	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.00	3.10	3.20
E	4.90	5.00	5.10
E2	3.00	3.10	3.20
e		0.50 BSC	
K	0.35	---	---
L	0.30	0.40	0.50
L3	---	---	0.10
L4		0.08 REF	

GENERIC MARKING DIAGRAM*

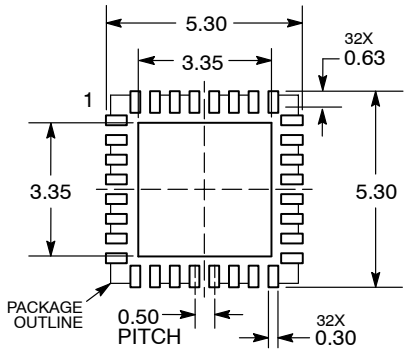


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON14940G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**QFNW32 5x5, 0.5P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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